

KAMPER

KT8942TX

MODEL

SERVICE MANUAL

TECHNICAL SPECIFICATIONS 11.1 CHASSIS

1. OPERATING CONDITIONS

POWER SUPPLY	140 TO 265 VAC
NOMINAL OPERATING VOLTAGE	230 VAC
TEMPERATURE RANGE	0 TO 45 DEGREES C
HUMIDITY RANGE	YEAR'S MEAN = 75% MAX = 95%

2. RF SECTION

2.1 RECEIVING CHANNELS FOR VHF/UHF BAND

	CCIR B/G	UK I	FRANCE L	OIRT D/K
VHF BAND				
BAND I		CHANNEL 2-4	CHANNEL 1-5	CH 2-4 CH 1-5
BAND III	CHANNEL 5-12	CHANNEL 6-12	CH 5-12	CH 6-12
CABLE	S1-S19, S20-S41	S1-S19, S20-S41	S1-S16, S21-S41	S1-S19-S22-S341

UHF BAND				
BAND IV-V	CHANNEL 21-69	CHANNEL 21-69	CH 21-69	CH 21-63

	MIN	NOM	MAX	UNIT
GAIN LIMITED SENSITIVITY				
INPUT SIGNAL LEVEL FOR				
STANDARD VIDEO OUTPUT VOLTAGE				
BAND 1/3	—	20	—	dB μ V
BAND 4/5	—	23	—	dB μ V
NOISE LIMITED SENSITIVITY				
INPUT SIGNAL LEVEL FOR 30 dB				
(S+N)/N-RATIO, WEIGHTED, CCIR				
REC 567				
BAND 1/3/4/5	—	30	—	dB (μ V)
SELECTIVITY HF+IF				
IF FREQUENCIES				
	B/G	I	L	D/M
Picture Carrier	38.9	38.9	38.9	38.9
Sound Carrier	33.4	32.9	32.4	32.4
Colour Carrier	34.47	34.47	34.47	34.47
VOLTAGE STANDING WAVE RATIO	MIN	NOM	MAX	UNIT
BAND 1/3	—	2	4	—
BAND 4/5	—	2	4	—
MAXIMUM INPUT SIGNAL LEVEL				
BAND 1/3		100 dB μ V (MAX)		
BAND 4/		100 dB μ V (MAX)		

3. VIDEO OUTPUT SECTION

	MIN	NOM	MAX	UNIT
VIDEO OUTPUT VOLTAGE				
(measured on cathode with				
lowest output level, contrast				
control and drive control at max	90	100	—	V
FREQUENCY RESPONSE				
INPUT AERIAL STANDARD, HF SIGNAL				
STANDARD B/G - D/K-I-L	-10	-7	—	dB
INPUT: SCART PIN 20				
STANDARD B/G - D/K-I-L		-8	-6	dB

4. CHROMA SECTION

PAL/SECAM	:	+-300	+-500	-	HZ
COLOUR CAPTURE RANGE	:				
PHASE ERROR OF REFERENCE	:	-	+-5	10	DEGRESS
CARRIER	:				
COLOUR KILLER	:	30			dB μ V (NOMINAL)

5. SOUND SECTION

	MIN	NOM	MAX	UNIT
SCART OUTPUT S/N RATIO	40	45	-	dB
NOISE LIMITED SENSITIVITY	:	38 db/V (NOMINAL)		
AM SUPPRESSION RATIO	:	60 db (NOMINAL)		
POWER OUTPUT (at 10% distortion) fm= 1KHz	:	3.0 or 4.0 Watts Rms (Mono Models) 2x7.0 Watts Rms (Stereo Models) 2x10.0 Watts Rms (Stereo Models)		

6. SYNCHRONISATION

LINE FREQUENCY LOCKING RANGE	:	± 300 HZ
VERTICAL FREQUENCY LOCKING RANGE	:	± 5 HZ

7. PICTURE TUBE DRIVE SECTION

EHT	:	25.0 \pm 0.5 KV
FOCUS VOLTAGE	:	MIN 25.6% MAX 38%
GRID 2 VOLTAGE RANGE	:	MIN 300 V, MAX 1350 V
HEATER VOLTAGE	:	6.2 \pm 0.2 Vms

Power Supply Voltages

B+ SUPPLY VOLTAGE (AT Ib=0)	28"	:	145V \pm 1V
	25"	:	145V \pm 1V
	21"	:	120V \pm 1V
	20"	:	121V \pm 1V
	14"	:	115V \pm 1V
20V OUTPUT Audio Stereo		:	20.0 \pm 0.5 VDC
12V OUTPUT Audio Mono		:	12 \pm 0.5 VDC
12V OUTPUT		:	12 \pm 0.5 VDC
8V OUTPUT		:	8.0 \pm 0.5 VDC
5V OUTPUT		:	5.0 \pm 0.5 VDC

8. OTHERS

AMBIENT OPERATING TEMPERATURE	:	0-45 DEGREES C
STORAGE TEMPERATURE	:	-10 TO + 85 DEGREES C
POWER CONSUMPTION 14"	:	75 Watts (max)
20"/21" Mono Models	:	95 Watts (max)
20"/21" Stereo Models	:	110 Watts (max)
25"/28"	:	135 Watts (max)
SAFETY	:	IEC 65 /BS P2N
X-RAY RADIATION	:	ACC. IEC 65 /BS P2N
Picture Tube Dimensions/Visible Screen Size	:	14" (37 cm/34 cm) 20" (51 cm/48 cm) 21" (55 cm/51 cm) 25" (63 cm/59 cm) 28" (70 cm/66 cm)

Triple video output amplifier

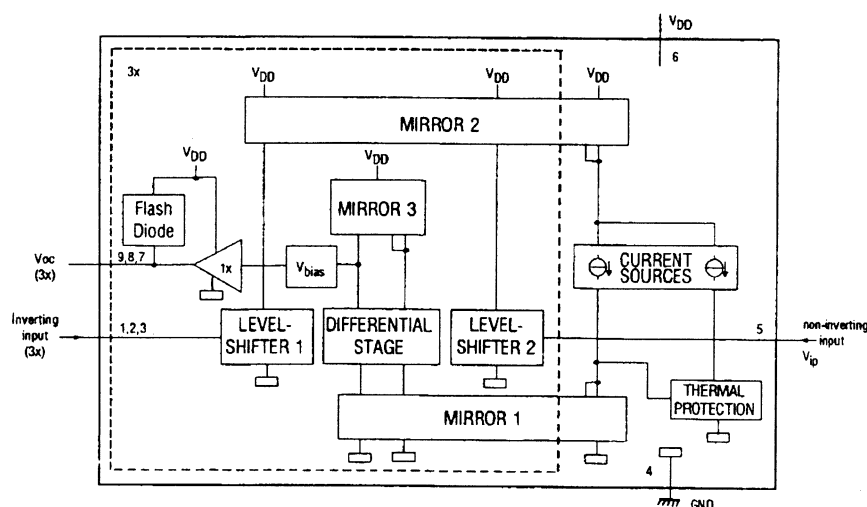
Features

- High bandwidth: 7.5 MHz typical; 60 V (peak-to-peak value)
- High slew rate: 1600 V/ μ s
- Simple application with a variety of colour decoders
- Only one supply voltage needed
- Internal protection against positive appearing Cathode-Ray Tube (CRT) flashover discharges
- One non-inverting input with a low minimum input voltage of 1 V

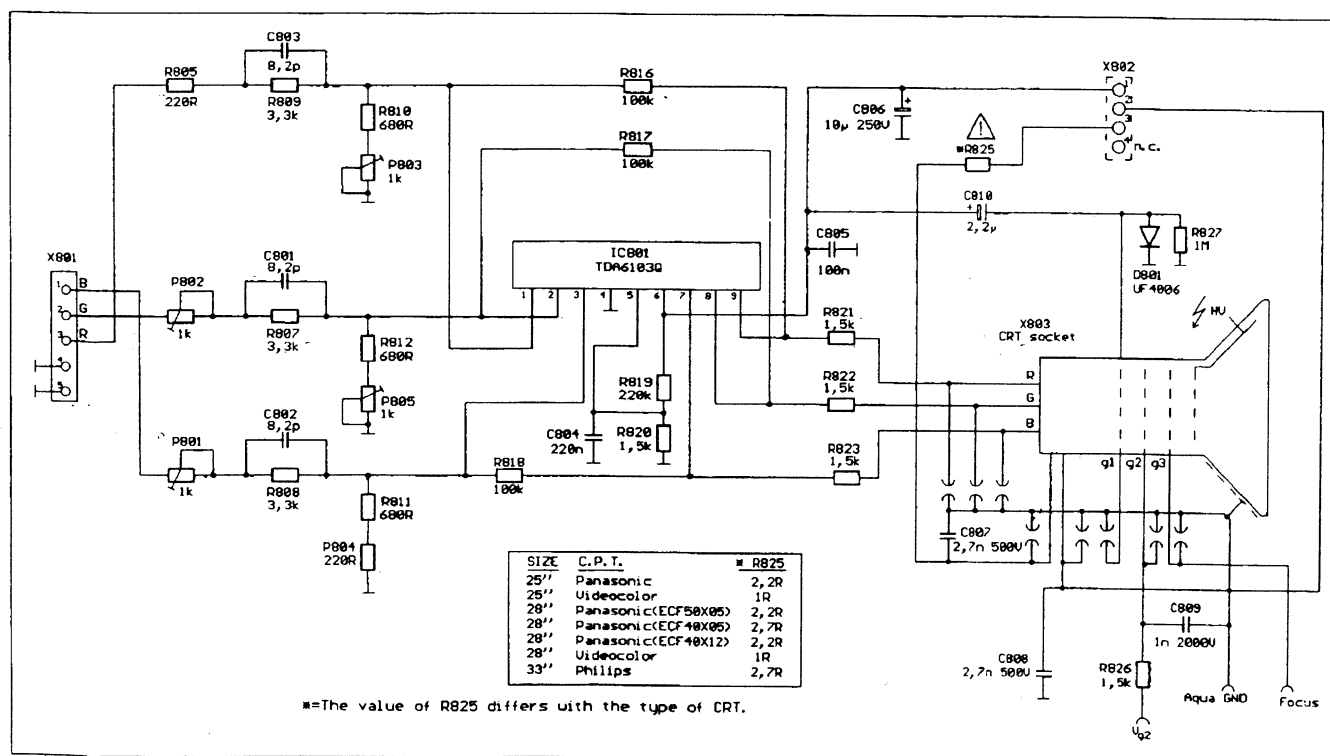
- Thermal protection
- Controllable switch-off behaviour.

General Description

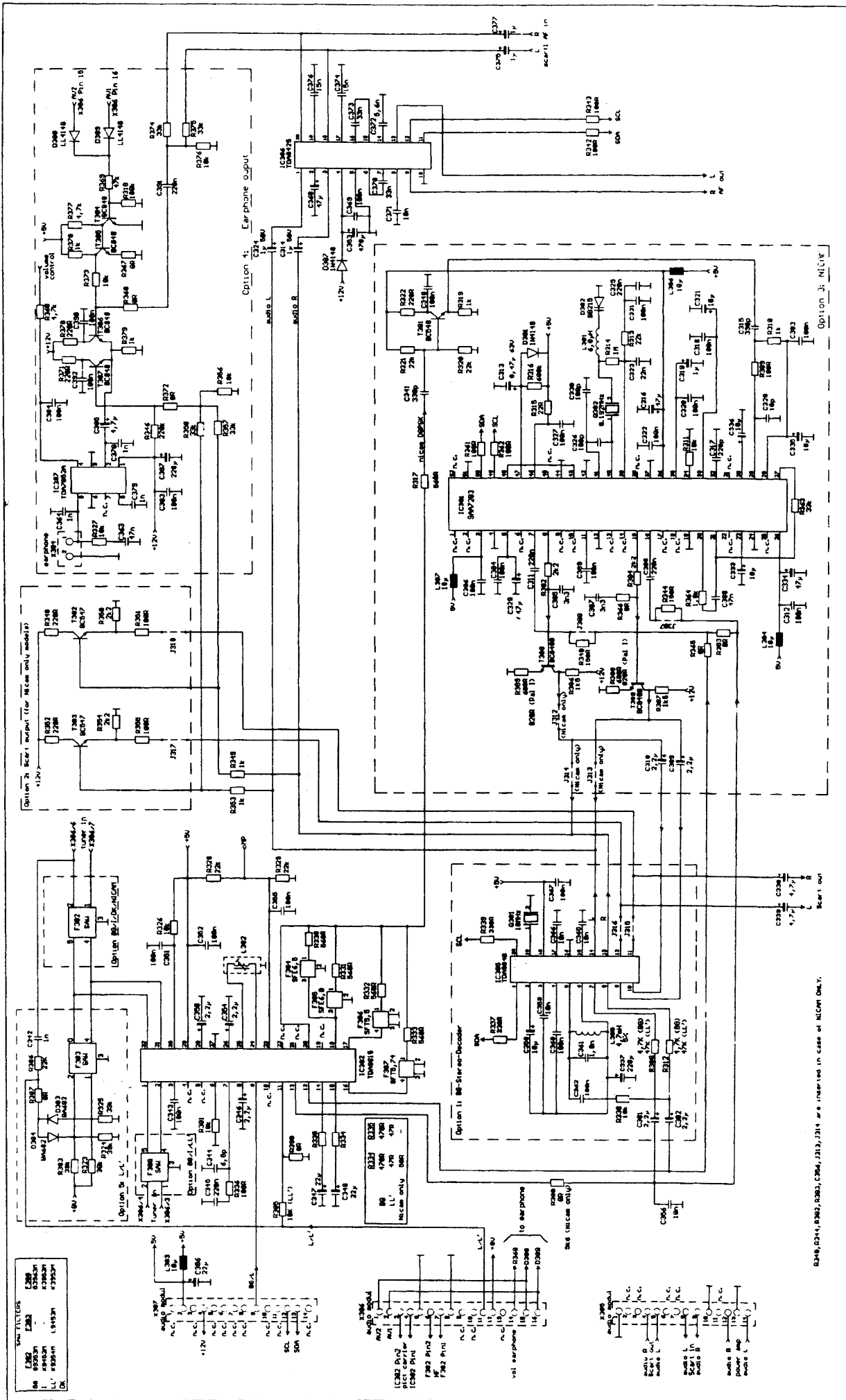
The TDA6103Q includes three video output amplifiers in one single in-line 9-pin medium power (SIL9MP) package SOT111BE, using high-voltage DMOS technology, intended to drive the three cathodes of a colour CRT.



Block Diagram (one amplifier shown).



Stereo/Nicom Module



Subject to change without notice

Circuit Description

In the period before the switch-on threshold is reached the IC is supplied via resistor **R1**; during the start-up phase it uses the energy stored in **C407** under steady state conditions the IC receives its supply voltage from transformer winding 5-6 via diode **D106**. The switching transistor **T401** is a BUZ 90. The parallel connected capacitor **C406** and inductance of primary winding 2-8 determine the system resonance frequency. The **R403**, **C405**, **D105** circuitry limits overshoot peaks, an **R102** protects the gate of **T401** against static charges.

During the conductive phase of the power transistor **T401** the current rise in the primary winding depends on the winding inductance and the mains voltage. The network consisting of **R413**, **C413** is used to create a model of the sawtooth shaped rise of the collector current. The resulting control voltage is fed into pin 2 of the IC. The RC-time constant given by **R413**, **C413** must be designed that way that driving the transistor core into saturation is avoided.

The ratio of the voltage divider **R414/R415** is fixing a voltage level threshold. Below this threshold the switching power supply shall stop operation because of the low mains voltage. The control voltage present at pin 3 also determines the correction current for the fold-back point. This current added to the current flowing through **R413**

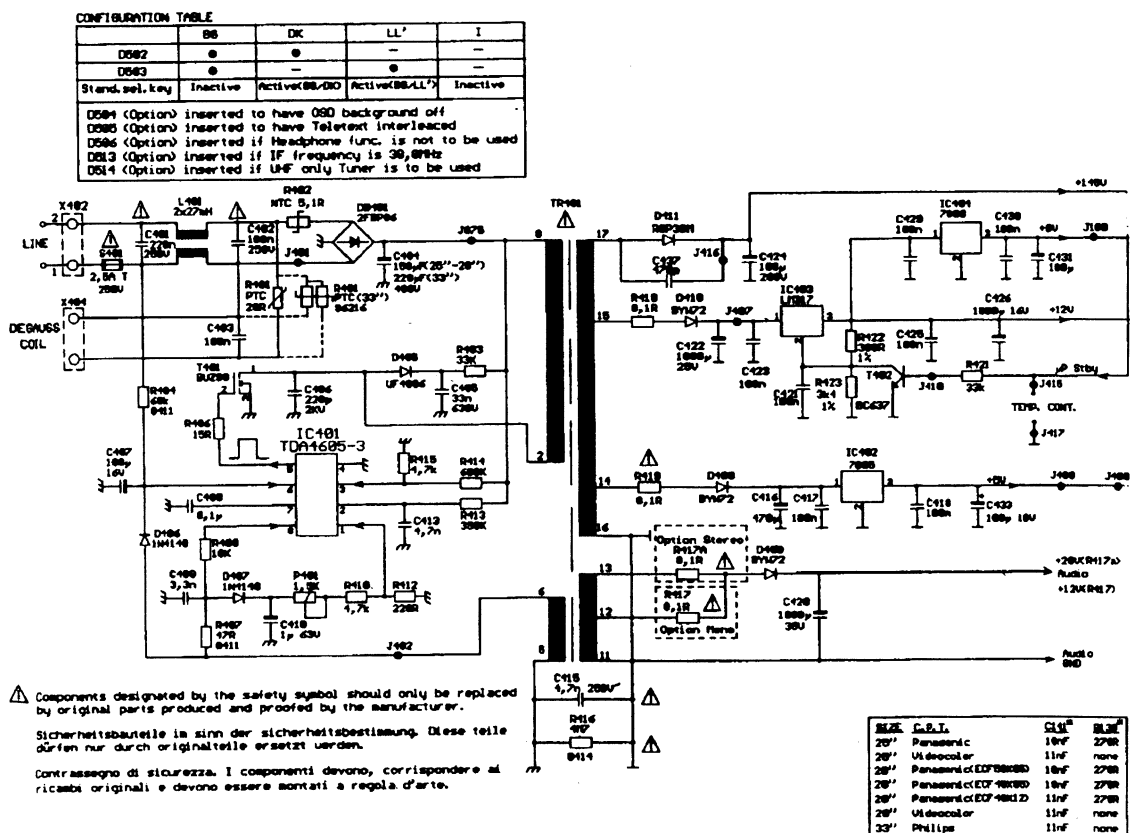
and represents an additional charge to **C413** in order to reduce the turn on phase of **T401**. This is done to stabilize the fold-back point even under higher mains voltages.

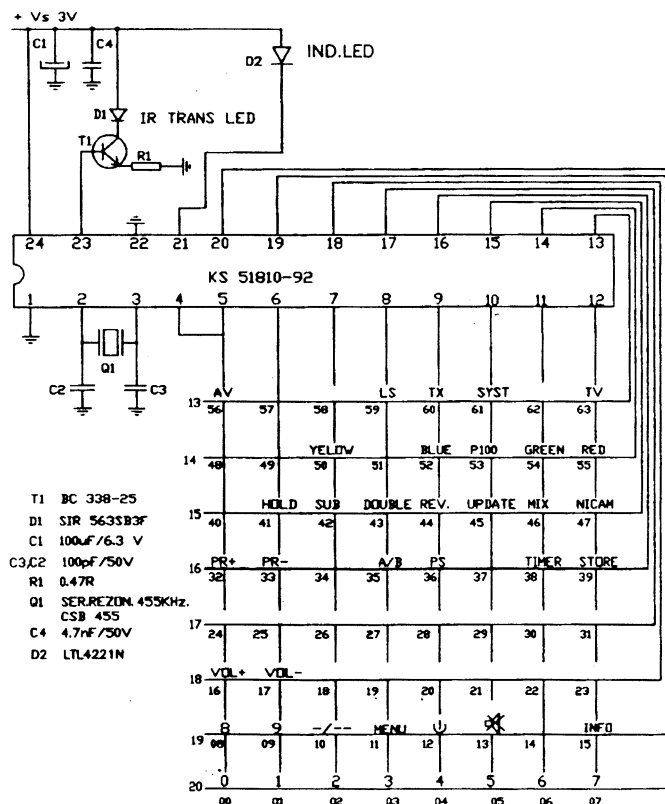
Regulation of the switched-mode power supplies via pin 1. The control voltage of winding 5-6 during the off period of **T401** is rectified by **D407** smoothed by **C410** and stepped down at an adjustable ratio by **R412** **R410** and **P401**. The **R407-C409** network suppresses parasitic overshoots (transformer oscillation). The peak voltage at pin 2, and thus the primary peak current, is adjusted by the IC so that the voltage applied across the control winding, and hence the output voltages, are at the desired level.

When the transformer has supplied its energy to the load, the control voltage passes through zero. The IC detects the zero crossing via series resistors **R408** connected to pin 8. But zero crossings are also produced by transformer oscillation after **T401** has turned off if output is short-circuited. Therefore the IC ignores zero crossings occurring within a specified period of time after **T401** turn-off.

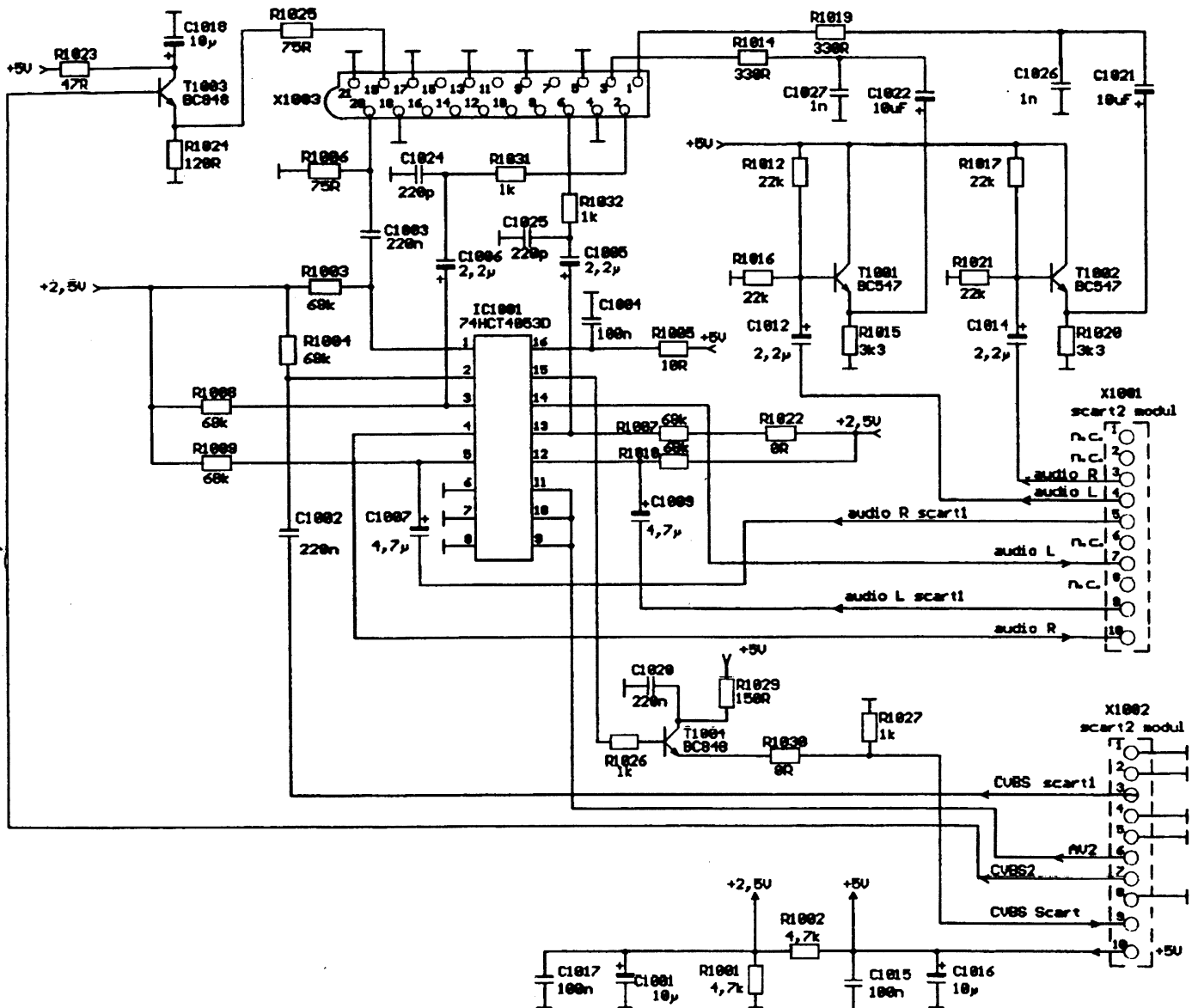
The capacitor **C408** connected to pin 7 causes the power supply to be started with shorter pulses to keep the operating frequency outside the audible range during start-up.

On the secondary side, the output voltages are produced across winding 11 to 17 rectified by **D411**, **D410**, **D409**, **D408** and smoothed by **C424**, **C422**, **C416**, **D420**.

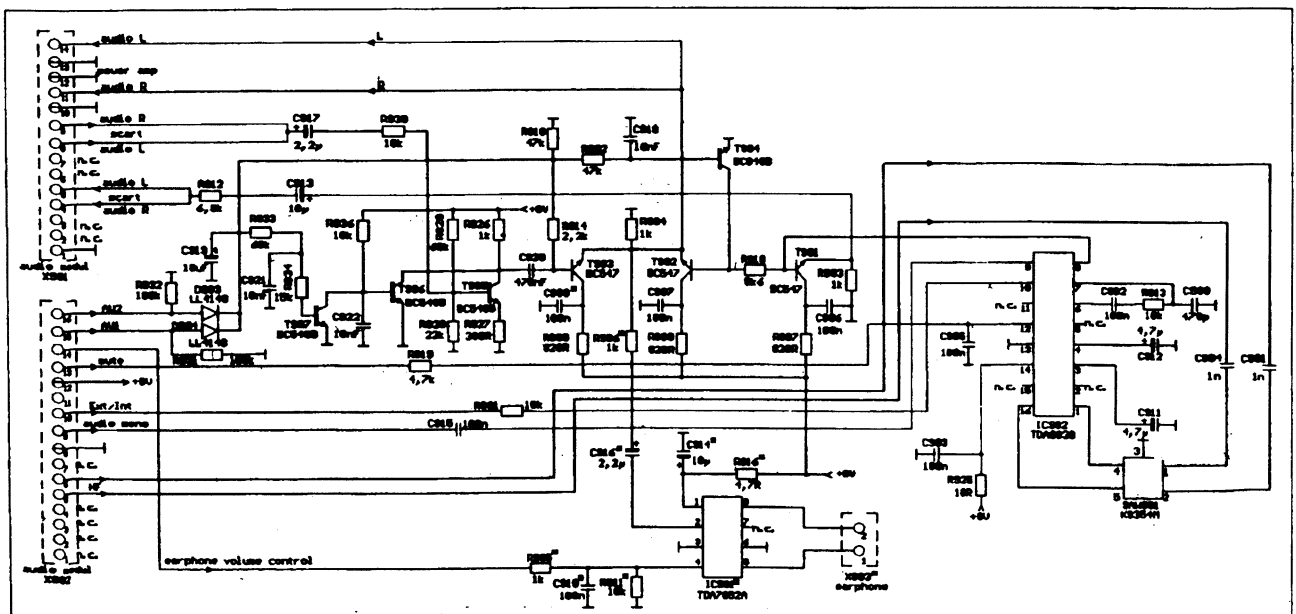




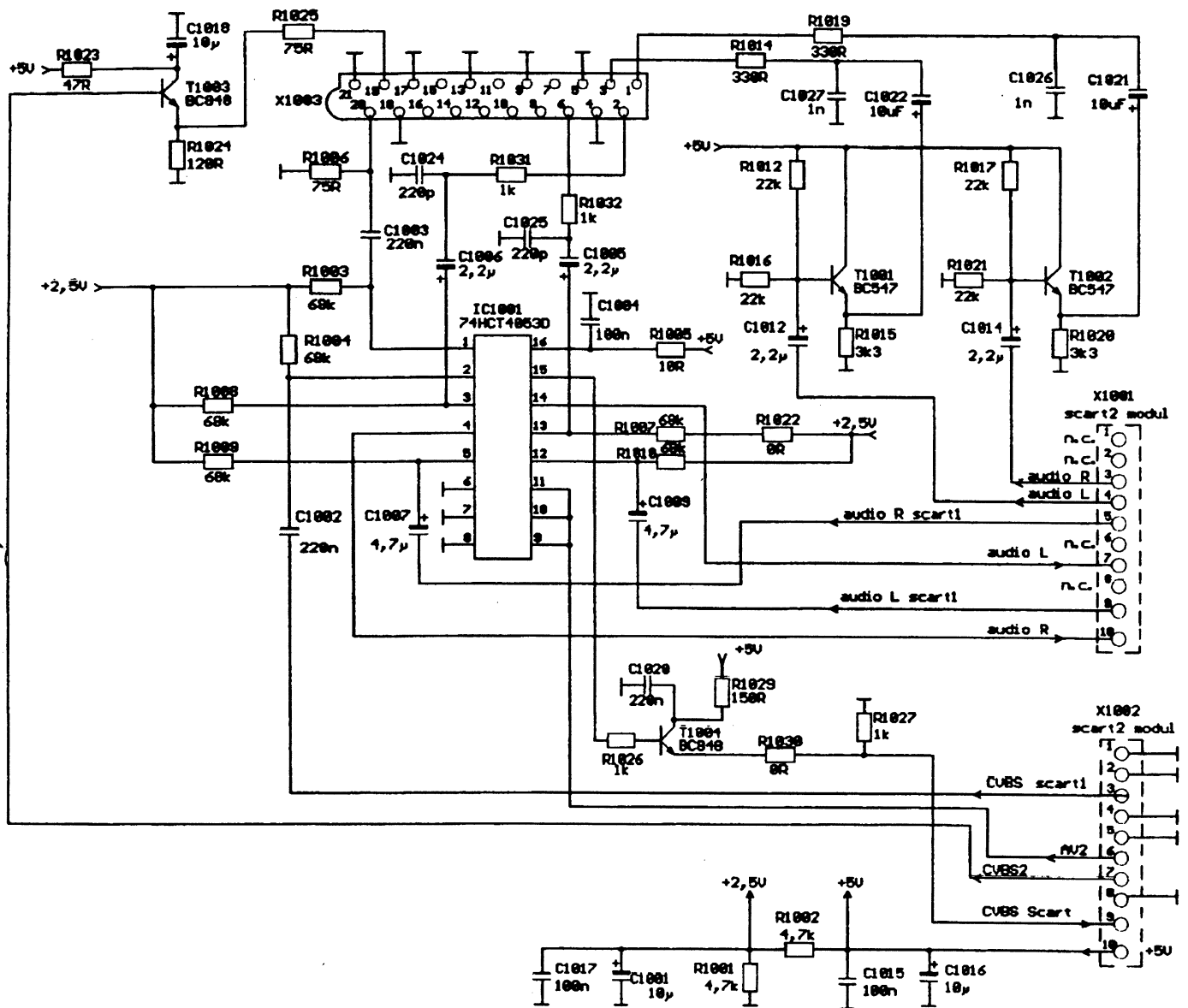
Double Scart Module



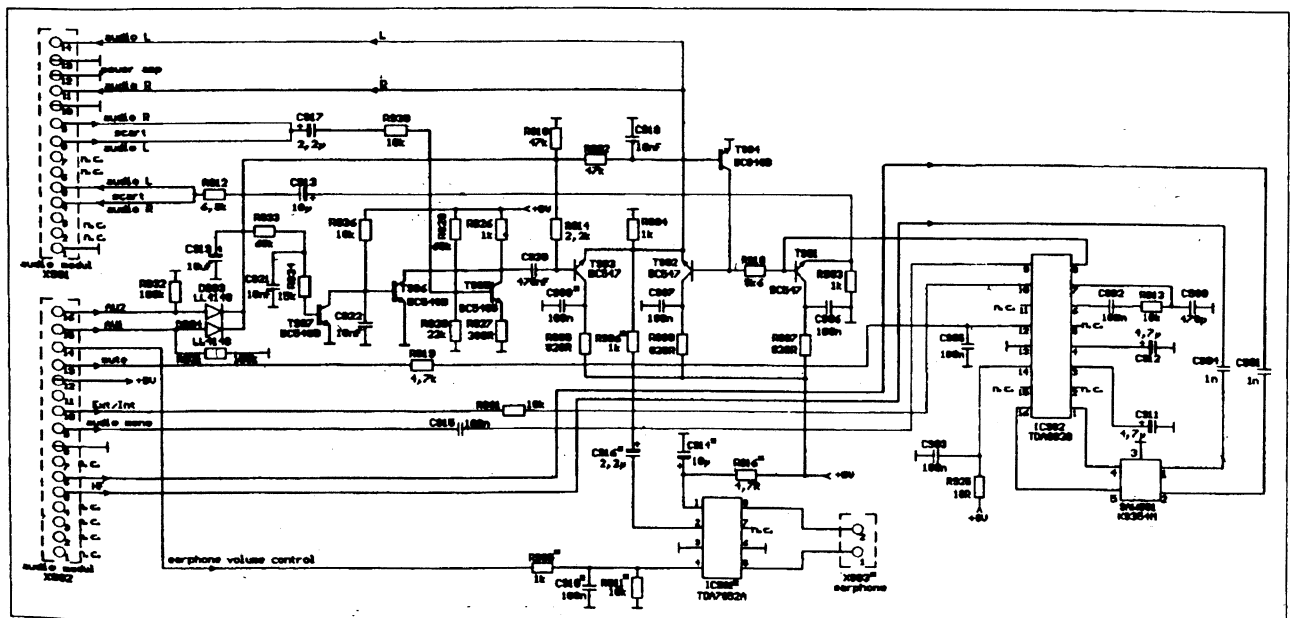
Secam L'am Module



Double Scart Module



Secam L'am Module



These components are Head Phone option

IC602
TDA7057AQ

External Speaker Outs
(option for 28')

1.8R
For 3W outputs
with one spkr.

1.5R
for 2=2W outputs.

0.47R
for 2=5W outputs.

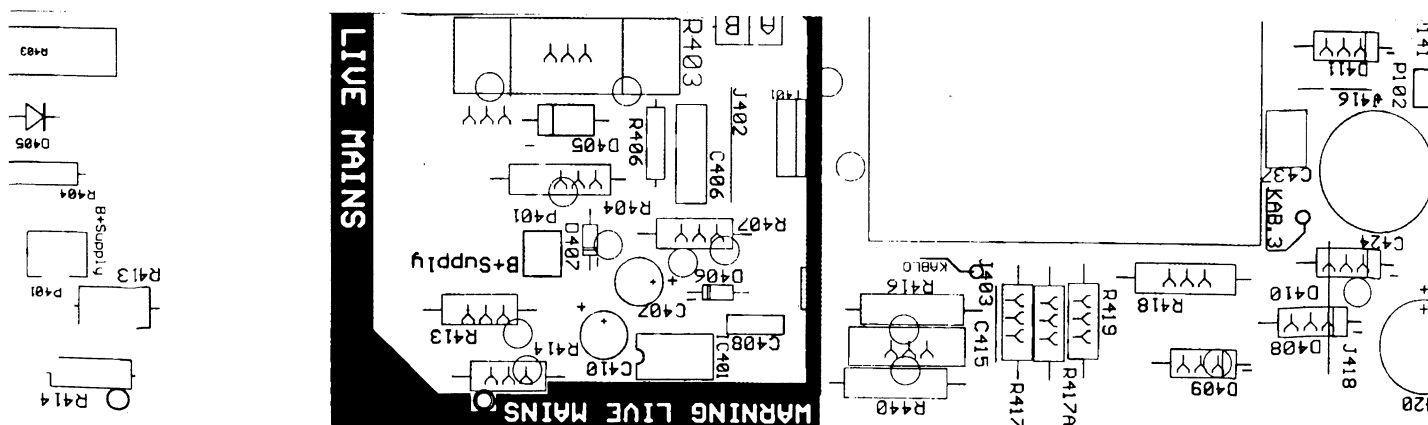
audio mono
From Sec LL
LAH Modul

audio mono
from C62

vol power amp
@P R502

C621, C622, C624, C625, C628 and C629 are EMC components.

MONO AUDIO POWER AMPLIFIER
AVAILABLE ON NON-STEREO MODELS
INSTEAD OF IC601-TDA1521

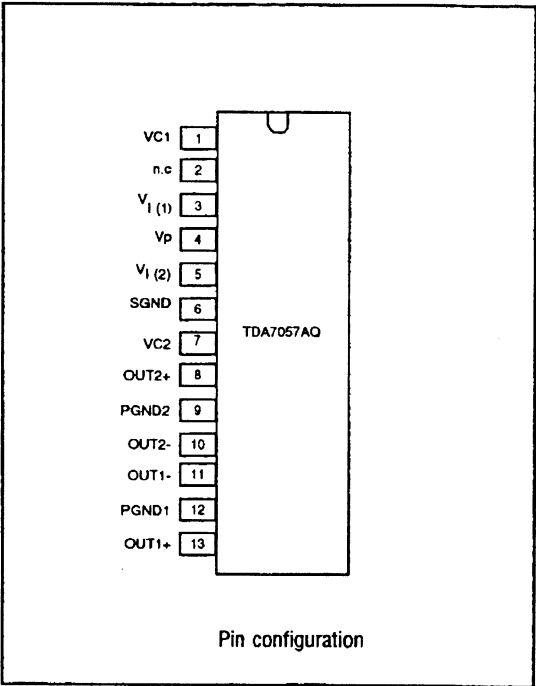


MAIN CHASSIS

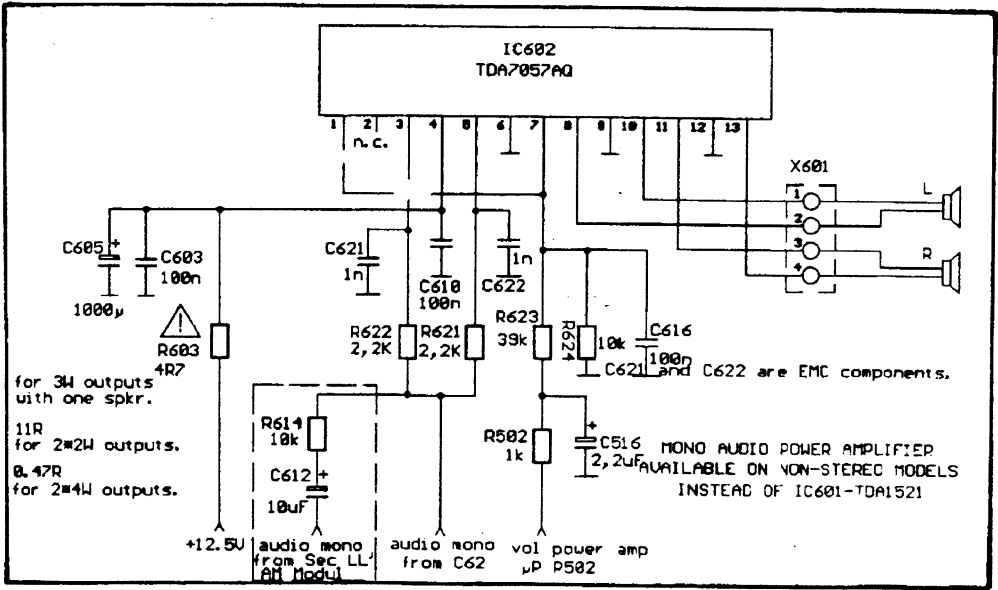
2 x 5 W setereo BTL audio output amplifier with DC volume control

Pinning

SYMBOL	PIN	DESCRIPTION
VC1	1	DC volume control 1
n.c	2	not connected
V _I (1)	3	voltage input 1
V _p	4	positive supply voltage
V _I (2)	5	voltage input 2
SGND	6	signal ground
VC2	7	DC volume control 2
OUT2+	8	positive output 2
PGND2	9	power ground 2
OUT2-	10	negative output 2
OUT1-	11	negative output 1
PGND1	12	power ground 1
OUT1+	13	positive output 1



Mono AF Power Module



TDA 8362 Multistandard TV Processor TDA 8361 Pal TV Processor

Vision IF amplifier, video demodulator, video amplifier, AGC and AFC are suitable for both negative and positive modulation.

Sound limiter, demodulator and amplifier with volume control.

Inputs and switches for external audio and CVBS signals.

Synchronization circuit with drive circuits for horizontal and vertical deflection.

Separate supply pin for starting the horizontal oscillator from the main rectifier.

X-ray protection (combined with the 2nd phase detector phase detector pin).

PAL/NTSC colour decoder in which the chroma filters (bandpass and trap) and the luminance delay line have been integrated. The circuit has a separate chroma input and the filters can be switched-off so that S-VHS signals (via an external switch) can be applied to the IC.

For SECAM applications an (alignment-free) SECAM-decoder can be added to the IC.

Peaking circuit in the luminance channel.

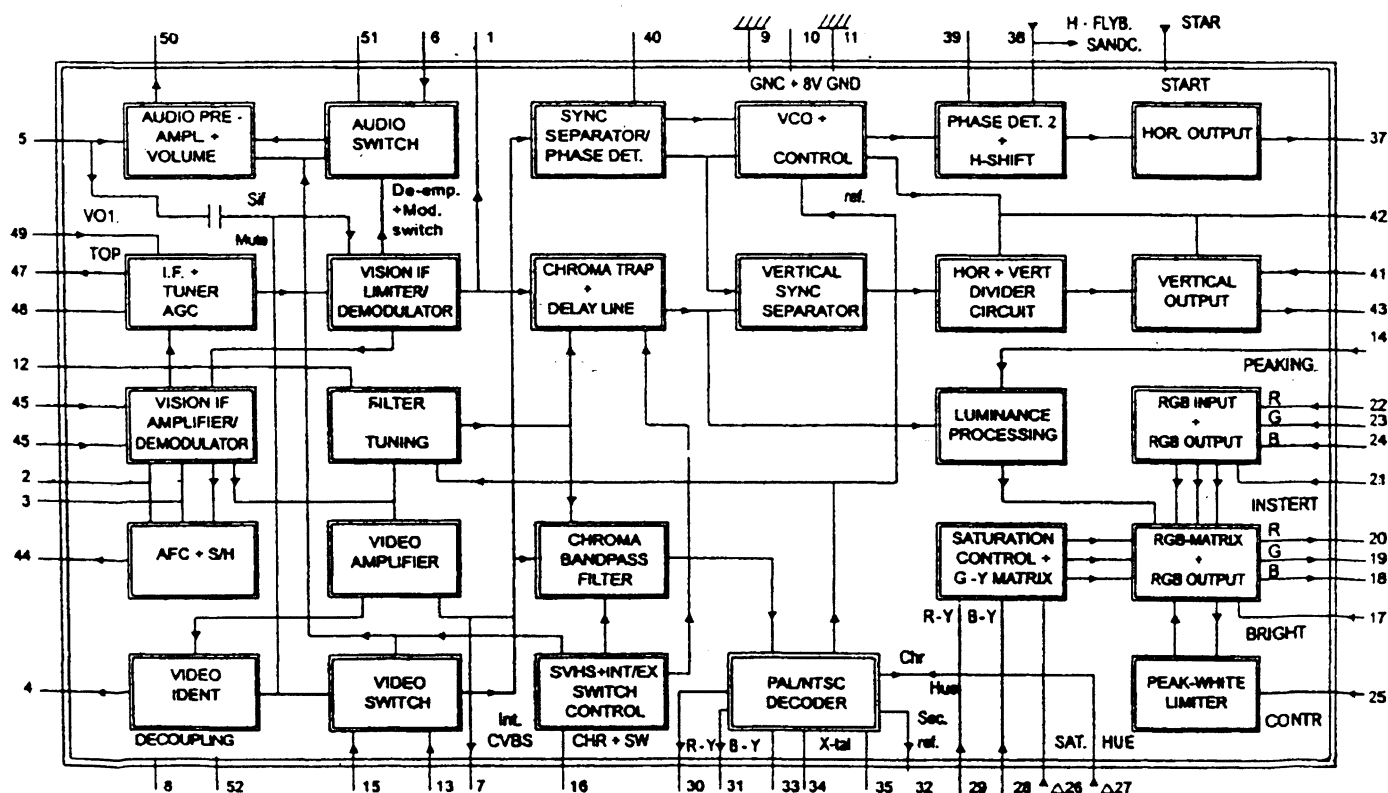
RGB-output circuit with linear inputs for On-Screen Character Display.

The supply Voltage for the IC is 8 Volts. It is mounted in an S-DIL envelope with 52 pins.

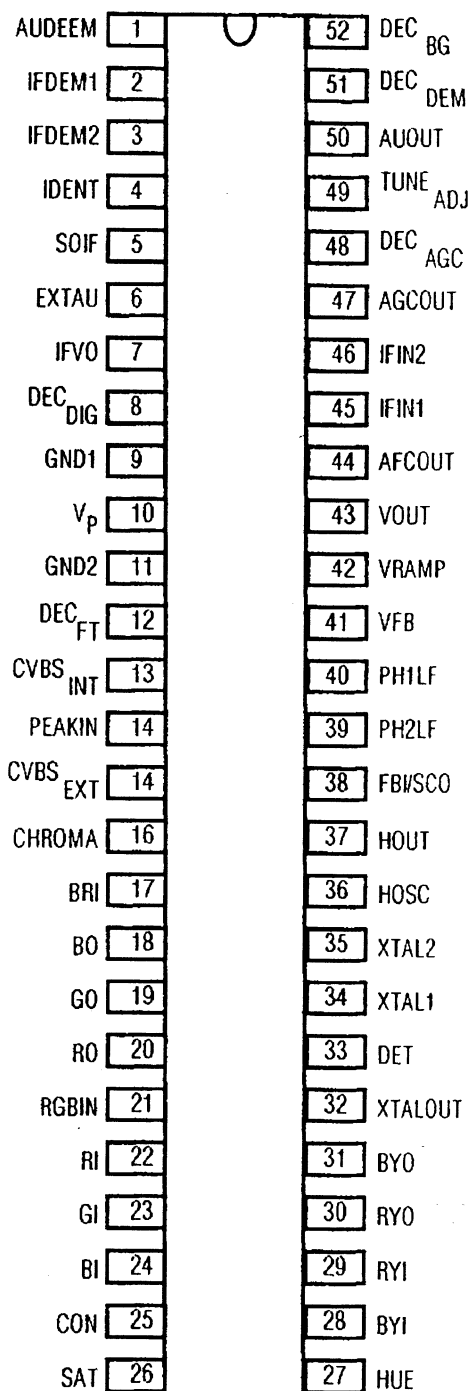
b) Features

- Multi-standard vision IF circuit (positive and negative modulation)
- Multi-standard FM sound demodulator (4.5MHz to 6.5 MHz)
- Video and audio switches (CVBS int/ext, S-VHS and audio int/ext)
- Integrated chroma trap and bandpass filters (auto-calibrated)
- Luminance delay line integrated
- PAL/NTSC colour decoder with automatic search system
- Easy interfacing with linear RGB inputs and fast blanking
- RGB-control circuit with linear RGB inputs and fast blanking
- Horizontal synchronization with two control loops and an alignment-free horizontal oscillator, vertical count-down circuit and a vertical pre-amplifier
- Low dissipation (only 600 mW)
- Small amount of peripheral components compared with completion IC's.
- Only one adjustment (vision IF demodulator)

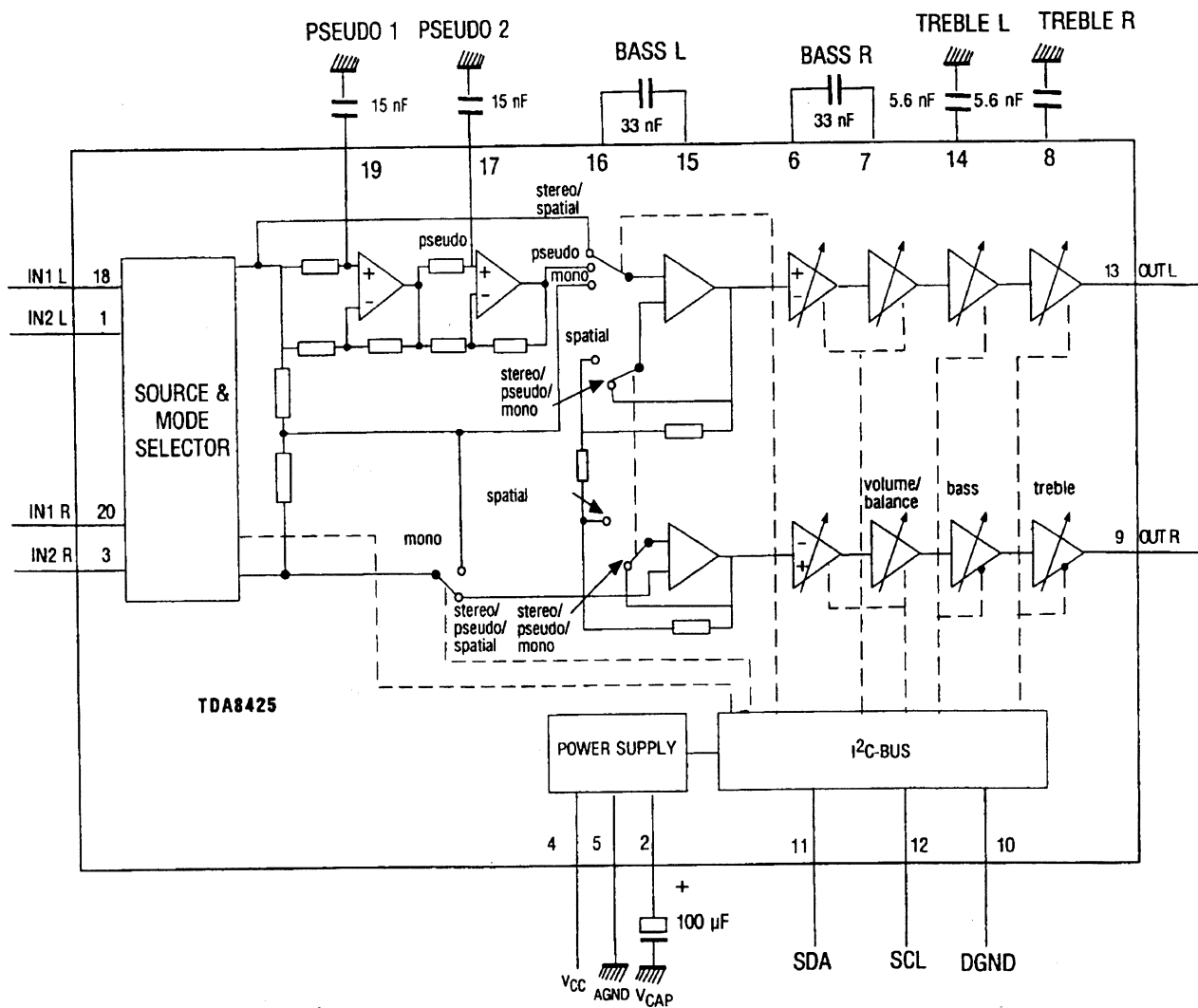
2) Block Diagram



SYMBOL	PIN	DESCRIPTION
AUDEMM	1	audio de-emphasis
IFDEM1	2	IF demodulator tuned circuit
IFDEM2	3	IF demodulator tuned circuit
IDENT	4	video identification output
SOIF	5	sound IF input and volume control
EXTAU	6	external audio input
IFVO	7	IF video output
DEC DIG	8	decoupling digital supply
GND1	9	ground 1
V	10	positive supply voltage (+8 V)
GND2	11	ground 2
DEC FT	12	decoupling filter tuning
CVBS INT	13	internal CVBS input
PEAKIN	14	peaking control input
CVBS EXT	15	external CVBS input
CHROMA	16	chrominance and A/V switch input
BRI	17	brightness control input
BO	18	blue output
GO	19	green output
RO	20	red output
RGBIN	21	RGB insertion and blanking input
RI	22	red input
GI	23	green input
BI	24	blue input
CON	25	contrast control input
SAT	26	saturation control input
HUE	27	hue control input (or chrominance output)
BYI	28	B-Y input signal
RYI	29	R-Y input signal
RYO	30	R-Y output signal
BYO	31	B-Y output signal
XTALOUT	32	4.43 MHz output for TDA8395
DET	33	loop filter burst phase detector
XTAL1	34	3.58 MHz XTAL connection
XTAL2	35	4.43 MHz XTAL connection
HOSC	36	start horizontal oscillator
HOUT	37	horizontal output
FBVSCO	38	flyback input/sandcastle output
PH2LF	39	phase 2 loop filter
PH1LF	40	Phase 1 loop filter
VFB	41	Vertical feedback input
VRAMP	42	Vertical ramp generator
VOUT	43	vertical output
AFCOUT	44	AFC output
IFIN1	45	IF Input 1
IFIN2	46	IF Input 2
AGCOUT	47	tuner AGC output
DEC	48	AGC decoupling capacitor
TUNE	49	tuner take-over adjustment
AUOUT	50	audio output
DEC Dem	51	decoupling sound demodulator
DEC BG	52	decoupling bandgap supply



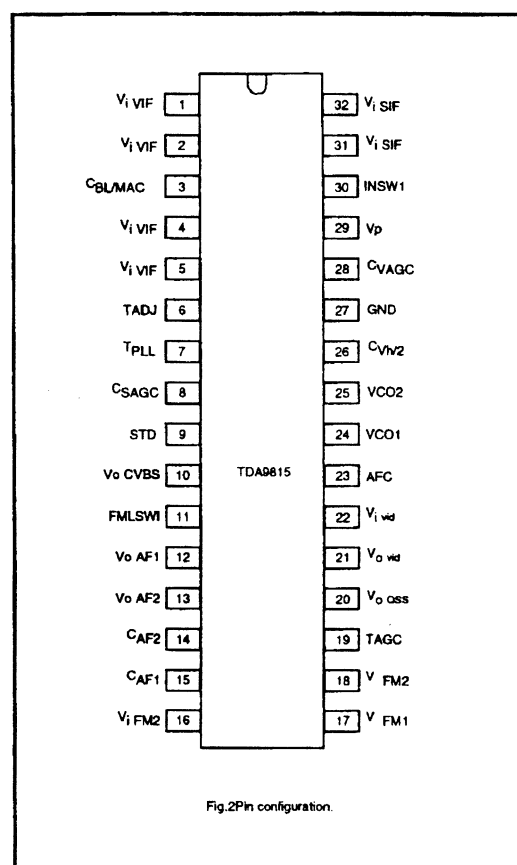
MBC203



Block Diagram

Pinning

SYMBOL	PIN	DESCRIPTION
Vi VIF	1	VIF differential input signal A
	2	
CBL/MAC	3	black level detector / MAC capacitor
Vi VIF	4	VIF differential input signal B
	5	
TADJ	6	tuner AGC takeover adjust (TOP)
TPLL	7	PLL loop filter
CSAGC	8	SIF AGC capacitor
STD	9	standard switch
Vo CVBS	10	CVBS output signal
FMLSW1	11	FM input select and L /L accent switch
Vo AF1	12	audio frequency output 1
Vo AF2	13	audio frequency output 2
CAF2	14	decoupling capacitor 2
CAF1	15	decoupling capacitor 1
Vi FM2	16	sound intercarrier input 2
Vi FM1	17	sound intercarrier input 1
Vi FM3	18	sound intercarrier input 3
TAGC	19	tuner AGC output
Vo OSS	20	single reference OSS output
Vo vid	21	composite video output
Vi vid	22	video buffer input
AFC	23	AFC output
VCO1	24	VCO reference circuit for 2fpc
VCO2	25	
Cvp/2	26	Vp/2 reference capacitor
GND	27	Vground
CVAGC	28	VIF AGC capacitor
Vp	29	positive supply voltage
INSWI	30	VIF input switch
Vi SIF	31	SIF differential input signal
	32	



Video buffer

For an easy adaption of the sound traps an operational amplifier with internal feedback is used in the event of B/G and L standard. This amplifier is featured with a high bandwidth and 7 dB gain.

SIF amplifier and AGC

The sound IF amplifier consists of two AC coupled differential amplifier stages.

Single reference QSS mixer

The single reference OSS mixer is realized by a multiplier. The SIF amplifier output signal is fed to the single reference OSS mixer and converted to intercarrier frequency by the regenerated picture carrier (VCO).

AM demodulator

The AM demodulator is realized by a multiplier. The modulated SIF amplifier output signal is multiplied in phase with the limited (AM is removed) SIF amplifier output signal.

FM detectors

Each FM detector consists of a limiter, an FM-PLL and a AF amplifier. The limiter provides the amplification and limitation of the FM sound intercarrier signal before demodulation.

- 1) The AF preamplifier for FM sound is an operational amplifier with internal feedback, high gain and high common mode rejection.
- 2) The AF output amplifier (10 dB) provides the required output level by means of a rail-to-rail output stage.

Internal voltage stabilizer and Vp/2-reference

The bandgap circuit internally generates a voltage of approximately 1.25 V, independent of supply voltage and temperature.

TDA9815 Multistandard/MAC VF-FLL with QSS-IF and dual FM-PLL/AM demodulator

General Description

The TDA9815 is an integrated circuit for multistandard vision IF signal processing (inclusive MAC) and sound AM- and Dual-FM demodulation, with single reference QSS-IF in TV and VTR sets.

Functional Description

Vision IF amplifier and input switch

The vision IF amplifier consists of three AC-coupled differential amplifier stages.

Tuner and VIF AGC

The AGC capacitor voltage is transferred to an internal IF control signal, and is fed to the tuner AGC to generate the tuner AGC output current on pin 19 (open-collector output). The AGC detector charges/discharges the AGC capacitor to the required voltage for setting of VIF and tuner gain in

order to keep the video signal at a constant level. The additional level information is given by the black level detector voltage.

Frequency-Phase detector (FPLL)

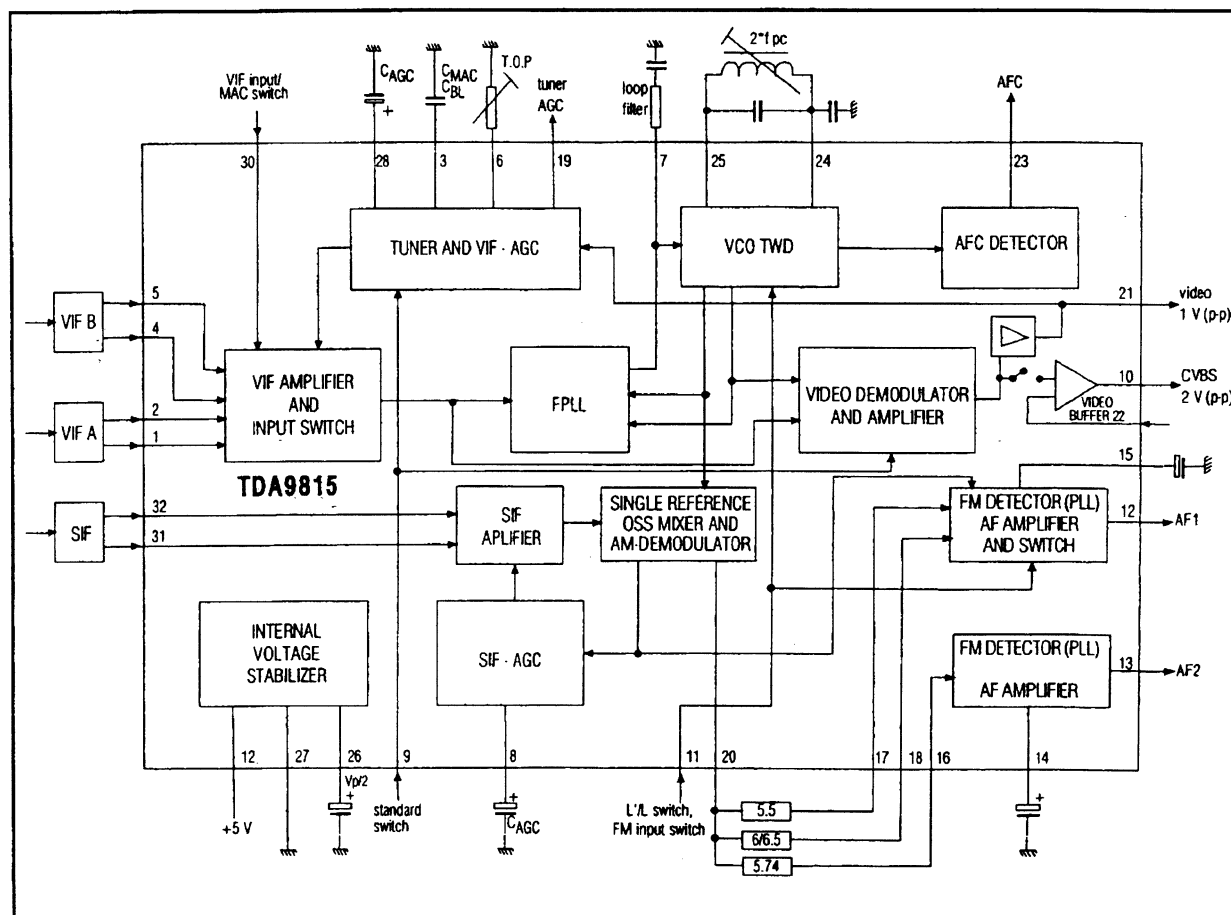
The VIF-amplifier output signal is fed into a frequency detector and into a phase detector via a limiting amplifier. In the event of positive modulated signals the phase detector is gated by composite sync in order to avoid signal distortion for overmodulated VIF signals.

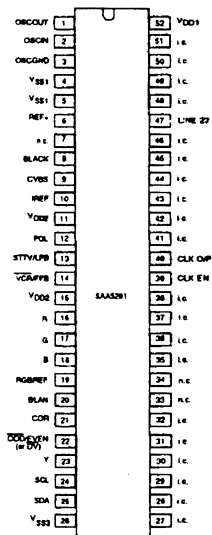
VCO, travelling wave divider and AFC

The VCO operates with a resonance circuit (with L and C in parallel) at double the PC frequency. The VCO is controlled by two integrated vercaps. Furthermore the VCO centre frequency can be decreased (required for L accent standard) by activating an additional internal capacitor. This is achieved by using the FM input and L accent switch pin 11.

Video demodulator and amplifier

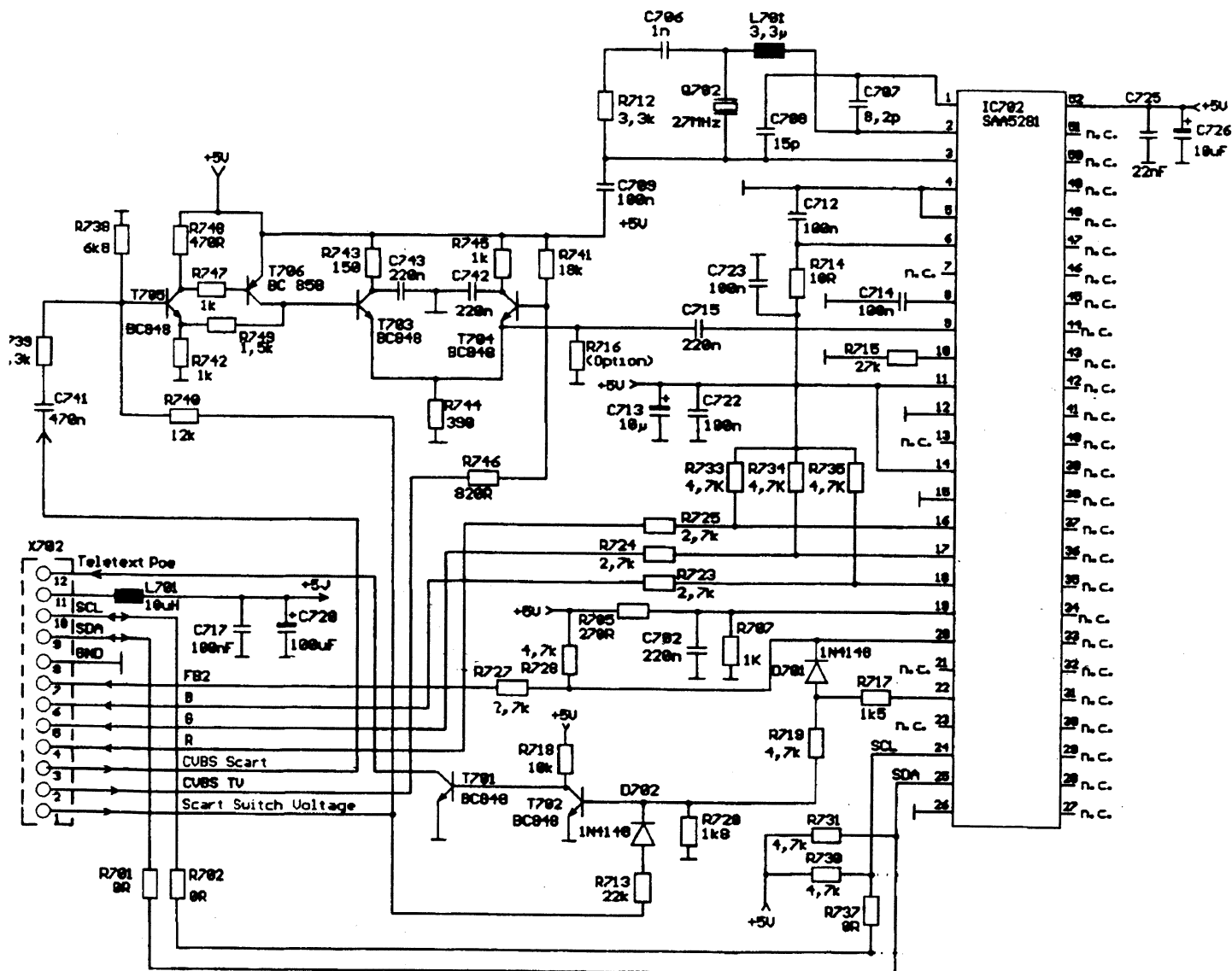
The video demodulator is realized by a multiplier which is designed for low distortion and large bandwidth.





Pin configuration; S

Type	Language					
SAA5281P/E	English	German	Swedish	Italian	French	Spanish
SAA5281P/T	English	German	Türkisch	Italian	French	Spanish
SAA5281P/H	Polish	German	Swedish	Serbo-croat	Czechoslovakia	Rumanian
SAA5281P/R	Estonian	Lettish /Lithuanian	Russian			
SAA5281P/K	French	Arabic				
SAA5281P/L	English	Hebrew	Arabic			



TELETEXT

SERVICE ADJUSTMENTS

1- Supply voltage adjustment

Adjust +B voltage, measured at the cathode of the diode D411, while screen potentiometer set to the minimum. For 28" to 145V \pm 1V

25" to 145V \pm 1V

21" to 120V \pm 1V

20" to 121V \pm 1V

14" to 115V \pm 1V

with P 401 potentiometer.

Set the screen potentiometer to a proper level to adjust the focus voltage.

2- IF 38.9 MHz adjustment

Apply an antenna signal with 60dB μ V \pm 1dB μ V (1mV) level to the set. Adjust L4 coil until the wave form shown on Fig. 1 at PIN of scart connector is received.

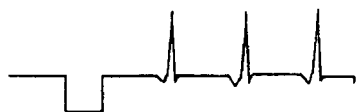


Fig 1

3- AGC Adjustment

Apply an antenna signal with 60dB μ V \pm 1dB μ V (1mV) level to the set. Observe the voltage at PIN 5 of tuner by adjusting P2 potentiometer. The voltage should be 9V-9,5V at maximum and should be adjusted below 1V.

4- Peaking or sharpness adjustment

Adjust the voltage at PIN14 of IC TDA8362 to 3.2V + 0,1V - 0,2V with P3 potentiometer. The RGB output signals at TDA8362 should have the same amplitude for cross-hatch test pattern.

5- Geometrie adjustments

Adjust the picture geometrie as follows;

with P1 horizontal position

with P104 vertical position

with P105 vertical amplitude

with P106 vertical linearity

6- East-west adjustments

Adjust the east west correction circuit as follows

with P101 trapez correction

with P102 horizontal amplitude

with P103 pin cushion correction

7- White Balance and Screen Adjustment

Turn the potentiometres P801, P802, P803, P805 to maximum. Adjust colour and contrast controls to minimum and brightness to medium level. Adjust the screen potentiometer to the level where flyback lines disappear while the screen is dark.

Adjust the white balance for high luminance level with P801 and P802 potentiometers, for low luminance level, with P803 and P805 potentiometer.

8- Stereo/Nicam Module Adjustment

Apply a stereo signal with L, 3kHz and R, 1kHz to the set. Turn the L302 coil upwards and observe the distortion on audio signal.

Turn the L302 coil downwards, adjust the voltage to 2,5 \pm V 0,1V at PIN 23 of IC302 while observing the 3kHz and 1kHz signals at audio output.

THE VALUES WILL BE PRESET ACCORDING TO THE TUBES:

White adjustment 9300 K (0)
High Light 60 Nits Low Light 6 Nits

1-) IRICO TUBE :

For a PAL Broadcast:

VER. AM. :15
VER. POS. :03
VER. LIN. :08
HOR. POS. :37

For a NTSC Broadcast:

VER. AM. :27
VER. POS. :04
VER. LIN. :08
HOR. POS. :37

RGB Values:

R-Gain :50
B-Gain :55
G-Gain :45
R-DC :45
G-DC :35

2-) PHILIPS TUBE :

For a PAL Broadcast:

VER. AM. :16
VER. POS. :02
VER. LIN. :10
HOR. POS. :37

For a NTSC Broadcast:

VER. AM. :26
VER. POS. :04
VER. LIN. :10
HOR. POS. :37

RGB Values:

R-Gain :50
B-Gain :55
G-Gain :45
R-DC :45
G-DC :35

3-) LG TUBE :

For a PAL Broadcast:

VER. AM. :19
VER. POS. :03
VER. LIN. :08
HOR. POS. :36

For a NTSC Broadcast:

VER. AM. :28
VER. POS. :04
VER. LIN. :08
HOR. POS. :36

RGB Values:

R-Gain :50
B-Gain :55
G-Gain :45
R-DC :45
G-DC :35

1-) SAMSUNG TUBE : 20"

For a PAL Broadcast:

VER. AM. :28
VER. POS. :01
VER. LIN. :33
HOR. POS. :45

For a NTSC Broadcast:

VER. AM. :45
VER. POS. :03
VER. LIN. :33
HOR. POS. :45

RGB Values:

R-Gain :50
B-Gain :55
G-Gain :45
R-DC :45

2-) LG TUBE : 20"

For a PAL Broadcast:

VER. AM. :25
VER. POS. :03
VER. LIN. :15
HOR. POS. :42

For a NTSC Broadcast:

VER. AM. :40
VER. POS. :05
VER. LIN. :15
HOR. POS. :42

RGB Values:

R-Gain :50
B-Gain :55
G-Gain :45
R-DC :45

These are the main values. Geometry and white adjustments will be corrected according to standards by entering the service mode when needed.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{IL} I_{IH}	Input Leakage Current	AFC Pin $V_{IH} = V_{DD}$ $V_{IL} = V_{SS}$ $V_{IH} = 12.0V$	-1		1 40	μA
I_{OH}	Output Leakage Current	DA0-DA5, PA4-PA5, PC0-PC7, O0, O1 $V_{OH} = V_{DD}$			10	μA
I_{OH}	Output Leakage Current High Voltage	DA0-DA5, PA4-PA7, PC4-PC7, O0, O1 $V_{OH} = 12V$			40	μA
I_{DD}	Supply Current RUN Mode	$f_{OSC} = 8MHz$, $I_{Load} = 0mA$ $V_{DD} = 6.0V$		6	16	mA
I_{DD}	Supply Current WAIT Mode	$f_{OSC} = 8MHz$, $I_{Load} = 0mA$ $V_{DD} = 6V$		3	10	mA
I_{DD}	Supply Current at transition to RESET	$f_{OSC} = \text{Not App.}$, $I_{Load} = 0mA$ $V_{DD} = 6V$		0.1	1	mA
V_{ON}	Reset Trigger Level ON	RESET Pin			$0.3 \times V_{DD}$	V
V_{OFF}	Reset Trigger Level OFF	RESET Pin	$0.8 \times V_{DD}$			V
V_{TA}	Input Level Absolute Tolerance	A/D AFC Pin $V_{DD} = 5V$			± 200	mV
V_{TR}	Input Level Relative Tolerance ⁽¹⁾	A/D AFC Pin Relative to other levels $V_{DD} = 5V$			± 100	mV

Note 1. Not 100% Tested

AC ELECTRICAL CHARACTERISTICS

($T_A = 0$ to $+70^\circ C$, $f_{OSC} = 8MHz$, $V_{DD} = 4.5$ to $6.0V$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{WRES}	Minimum Pulse Width	RESET Pin	125			ns
t_{OHL}	High to Low Transition Time	PA6, PA7 $V_{DD} = 5V$, $CL = 100pF$ ⁽²⁾		100		ns
t_{OHL}	High to Low Transition Time	DA0-DA5, PB0-PB6, OSD Outputs, PC0-PC7 $V_{DD} = 5V$, $CL = 100pF$		20		ns
t_{OLH}	Low to High Transition Time	PB0-PB6, PA0-PA3, OSD Outputs, PC0-PC3 $V_{DD} = 5V$, $CL = 100pF$		20		ns
f_{DA}	D/A Converter Repetition Frequency ⁽¹⁾			31.25		kHz
f_{SIO}	SIO Baudrate ⁽¹⁾			62.50		kHz
t_{WEE}	EEPROM Write Time	$T_A = 25^\circ C$ One Byte		5	10	ms
Endurance	EEPROM WRITE/ERASE Cycles	Q_A Lot Acceptance Criteria	300,000	> 1 million		cycles
Retention	EEPROM Data Retention ⁽⁴⁾	$T_A = 25^\circ C$	10			years
C_{IN}	Input Capacitance ⁽³⁾	All Inputs Pins			10	pF
C_{OUT}	Output Capacitance ⁽³⁾	All Outputs Pins			10	pF
COSCin, COSCout	Oscillator Pins Internal Capacitance ⁽³⁾			5		pF
COSDin, COSDout	Oscillator Pins External Capacitance ⁽³⁾	Recommended	15		25	pF

Notes:

1. A clock other than 8MHz will affect the frequency response of those peripherals (D/A, and SPis) whose clock is derived from the system clock.
2. The rise and fall times of PORT A have been increased in order to avoid current spikes while maintaining a high drive capability
3. Not 100% Tested
4. Based on extrapolated data

FUNCTIONAL DESCRIPTION

1 - DEFLECTION CIRCUIT

Note : [X,Y] : line number referred to the internal line counter numbering

- Fully integrated synch. separator, with a low pass filter, a black level alignment of the Y/CVBS input, a slicing level at 2/3, 1/3 of the sync. pulse amplitude.
- Frame sync. pulse locked on $2 f_H$ frequency to perfect interlace.
- 500kHz VCO with an external ceramic resonator.
- Two phase locked loops
 - ∞ the first PLL locks the VCO on the video signal frequency,
 - ∞ the second PLL compensates the line transistor storage time.
- Three time constants for the first PLL.
 - ∞ the long time constant is used for normal operation
 - ∞ the short time constant is automatically used during the frame retrace and in search mode of VCR when the frame pulse is outside [258,264] and [309,314].
 - ∞ very long time constant when no video recognition

Time constants in normal operation
(automatic selection of time constants) :

50Hz input signal :

- short time constant : [306, 21]
- long time constant : the rest of the field

∞ inhibition of the first PLL :

the first locked loop is opened from line 309 to line 4.5 (or 314) in 50Hz mode.

∞ the time constants values are chosen by means of external components.

∞ possibility to force the short time constant through the bus.

∞ possibility to force the very long time constant through the bus.

- Video identification : coincidence detector between the line synchro top and a line frequency window from the first PLL. The video identification status is available in the output register of the I²C bus decoder.
- Generation of burst gate pulses and line frequency signals from the first PLL to drive the chroma and video circuits. The burst gate pulse is also sent to the sandcastle generator.
- Frame synchro window :
[248, 352] catching
- Field frequency selection windows :
[288, 352] 50Hz mode selection window
- frame blanking pulse :
from line 0 to 21 in 50Hz mode
- Vertical output pulse is 10.5 lines long.
- Horizontal output pulse : 28μs line pulse on an open collector output;
- Start up circuit : the horizontal output is at a high level when V_{CC} increases from 0 to 6.8V. On shutting down, horizontal pulses are disabled when V_{CC} is below 6.2V.

- Soft-start circuit : the duty cycle of the horizontal output is 78 % (Thigh/(Thigh + TLow)) when V_{CC1} is lower than (0.75 x V_{CC2}), during the rising time.

During the falling time, a 78% duty cycle HOUT pulse is provided when V_{CC1} is lower than (0.60 x V_{CC2}).

- Possibility to disable the horizontal output pulse through the bus (force a high level on HOUT).
- Horizontal position adjustment controlled by bus.
- Bus controlled output voltage to adjust the vertical amplitude; this voltage permits to adjust the slope of the vertical sawtooth generated by the external frame booster.
- Bus controlled vertical position ; the high level of the vertical pulse permits to adjust the vertical position.
- Bus controlled 4/3-16/9 selection : the low level of the vertical pulse is 0.1V when 16/9 is selected, 2V when 4/3 is selected.

- Combined flyback input and sandcastle output (Pin 37).

Two thresholds on LFB/SCO Pin : The lowest threshold (0.7V) permits to extract the line blanking pulse; the highest threshold (2V) permits to extract the line pulse for PLL2.

The sandcastle signal at Pin 37 is used to control the external baseband chroma delay line.

FUNCTIONAL DESCRIPTION (continued)

2 - FILTERS

- Integrated trap filter :

$$Q = \frac{1}{\frac{f_o}{f_{-3dB}} - \frac{f_{-3dB}}{f_o}}$$

Q = 1.7 at sharp. min
Q = 3.0 at sharp. max

Center frequency : - 4.43MHz for PAL

- 4.25MHz, for SECAM

(f_{-3dB} = 3MHz ; -20dB rejection between 4.1MHz and 4.4MHz)

- Integrated chroma bandpass :

Q = 3.5

Center frequency : 4.43MHz, 3.58MHz

- Integrated cloche filter for SECAM :

Q = 16

Center frequency : 4.286MHz

- Integrated delay line :

Bandwidth = 8MHz

- Integrated low pass filter for deflection part.

- All filters are tuned with a reference phase locked loop.

^{3/25}
The PLL consists of a lowpass filter, a phase comparator, a loop filter (with an external capacitor). The reference signal is the continuous carrier wave from the VCO (4.43MHz).

The PLL adjusts the center frequency of the lowpass so that it is equal to the reference signal. The tuning voltage of the PLL is used to adjust all other filters.

The cloche filter is fine tuned with a second PLL operating during frame retrace.

3 - VIDEO CIRCUIT

- 2 RGB inputs : RGB (OSD) input has priority against the RGBext. Maximum contrast on RGB (OSD). -10dB range contrast control on RGBext. Possibility to disable the RGBext insertion through the bus.
- Oversize blanking capability on FB(OSD)(Pin15) input. The RGB outputs will be blanked when the voltage on Pin 15 will exceed the second threshold at 1.9V (blanking threshold) : the whole field is blanked but not the inserted cut-off pulses. The OSD insertion threshold is 0.7V.
- Automatic cut-off current loop : 2V cut-off range. Sequential cut-off current measurement during the three lines after the frame blanking signal. Leakage current measurement during the frame blanking, memorization on an internal capacitor.
- Warm up detector.
- Beam current limiter DC voltage input. The beam current limiter control voltage will act on contrast first, then the brightness will be decreased when contrast attenuation reaches -5dB.
- Bus control of the red, green and blue channel gain (White point adjustment)
- Bus control of the red and green DC levels (black point adjustment)
- PAL and SECAM matrix).
- Switch-off of the trap filter in SVHS mode.
- Bus controlled contrast on luminance (20dB range)
- Bus controlled saturation (50dB range)
- Bus controlled brightness : 40% range at maximum contrast.
- Bus controlled sharpness (peaking) ; sharpness active in PAL standard only.
- Noise coring function on sharpness.

FUNCTIONAL DESCRIPTION (continued)

4 - CHROMA CIRCUIT

4.1 - PAL/SECAM Decoders

- SVHS inputs ; bus controlled SVHS mode.
- 30dB range ACC
- Use of an external base band delay line (STV2180 recommended)
- Automatic standard identification, with possibility to force the standard through the bus.

4.2 - PAL Decoder

- ACC done by peak detector on synchronous demodulation of the burst
- Fully integrated killer functions.
- VCO using two standard crystals : 4.43MHz and 3.58MHz.
3.58MHz crystal is temporarily requested on this version to achieve proper standard identification.

XTAL SPECIFICATION :

Frequency :

4.433619MHz (PAL/SECAM)

Vibration mode : Fundamental, series resonance (no serial capacitor)

Motional capacity : 13fF \pm 3fF

Resonance resistance : < 70 Ω

Shunt capacitance : < 7pF

Spurious response : No resonance at $3 \cdot f_0 \pm 3\text{kHz}$

- 0° and $\pm 90^\circ$ demodulation angles for PAL

4.3 - SECAM Decoder

- ACC
- Fully integrated killer
- Two integrated discriminators with two PLL
- Integrated deemphasis

4.4 - Standard Identification

- Sequential identification.
- 3 identification sequences : XTAL1 (4.43MHz) mode to identify PAL, XTAL2 (3.58MHz) mode not used, SECAM mode (XTAL1 selection).
- PAL priority
- the SECAM mode is locked after two identified SECAM sequences
- the SECAM mode can be selected in 50Hz only
- Blanking of the (R-Y) and (B-Y) outputs during color search mode.

5 - OTHER FUNCTIONS : IF CONTROLS

5.1 - Volume Control and Mute

The volume control voltage range on Pin 10 is from 0.5V to 5V. A low voltage on Pin 10 (below 0.2V) will mute the FM demodulator of the IF circuit STV8224. It will put the volume at the minimum level and thus there will be no sound either in TV mode or SCART mode.

The volume control voltage and the mute level are controlled by the bus.

5.2 - IF Standard and TV/SCART Mode Selection

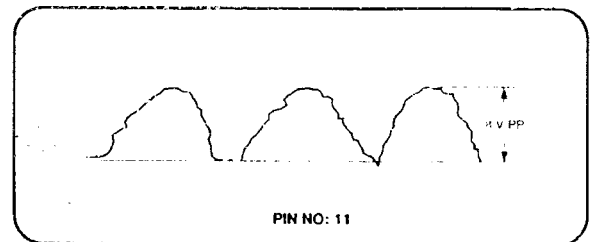
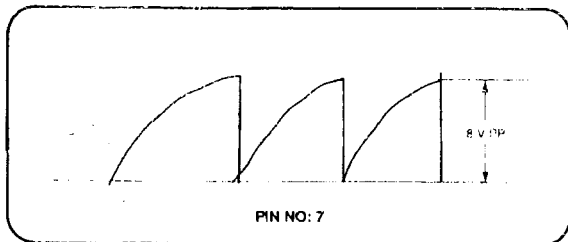
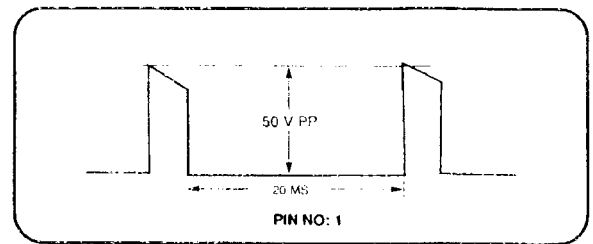
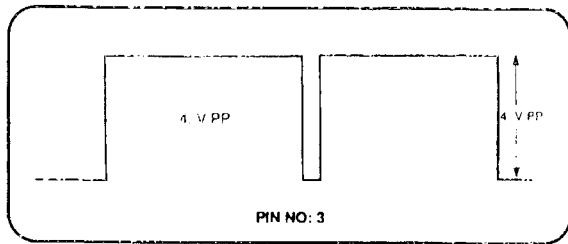
The selection of IF standard (positive or negative vision modulation) and the TV/SCART mode is controlled by the bus. The selection is converted in four voltages on Pin 21.

The lowest voltage selects the TV mode and the NEGATIVE vision modulation.

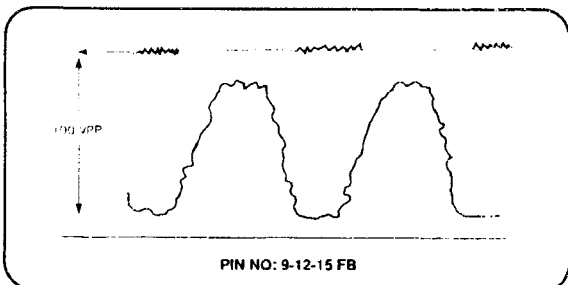
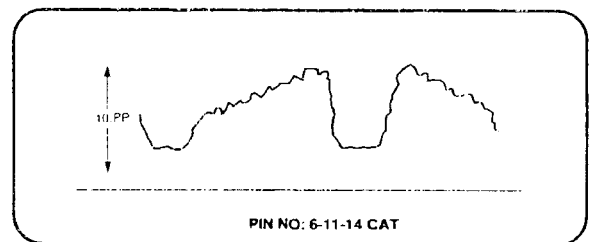
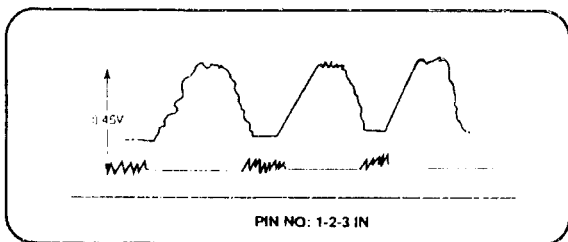
The highest voltage (open collector output with internal pull-up resistor to V_{CC}) selects the SCART mode and the NEGATIVE vision modulation.

The two other intermediate voltages select either TV mode and POSITIVE vision modulation or SCART mode and POSITIVE vision modulation.

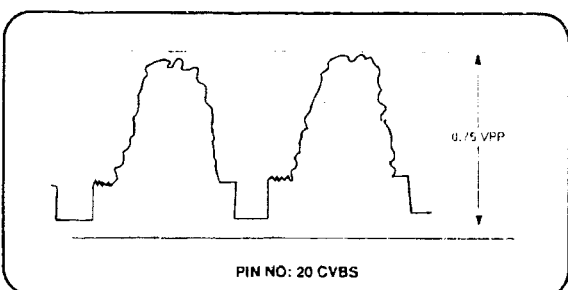
**IC501 TDA 8174A
OSCILLOSCOPE WAVE FORMS**



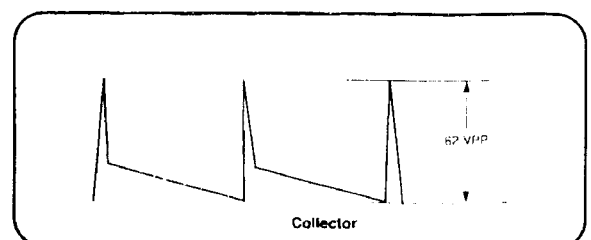
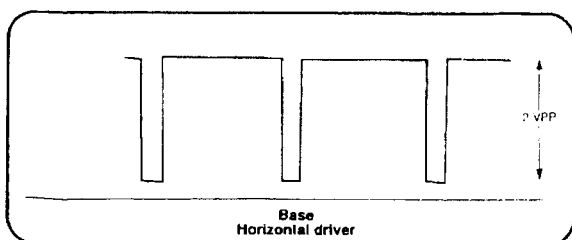
**IC801 STV5112
OSCILLOSCOPE WAVE FORMS**



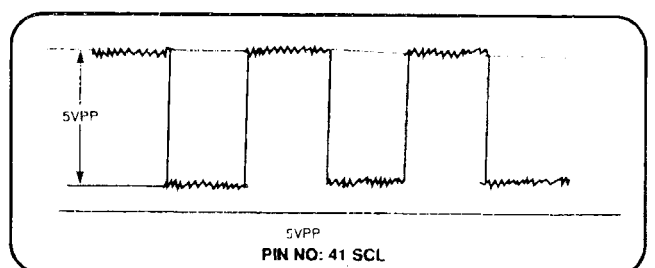
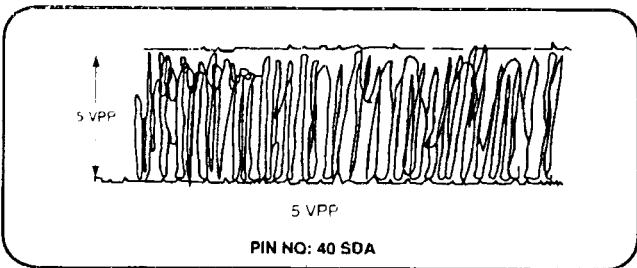
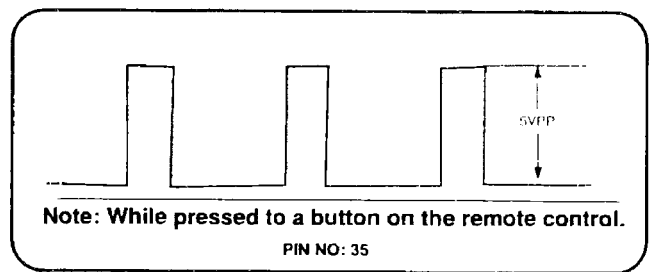
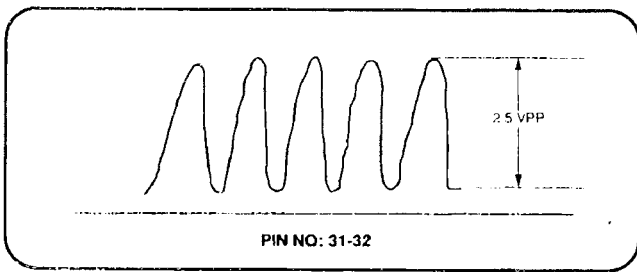
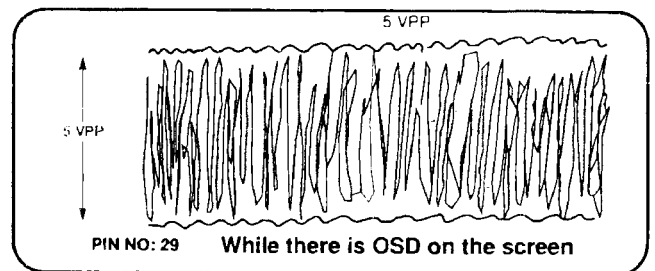
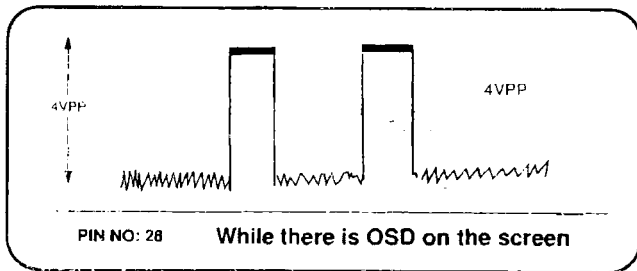
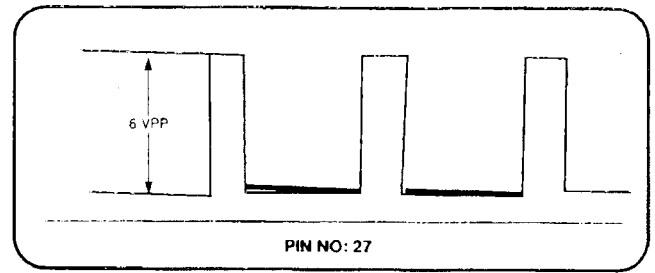
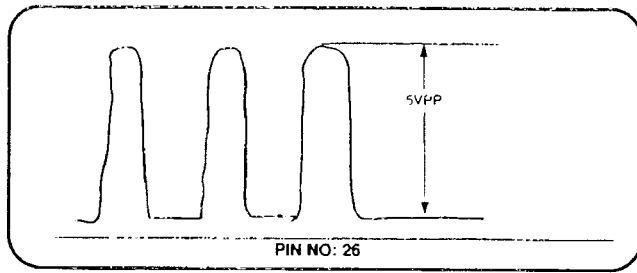
**IC151 STV2116A
OSCILLOSCOPE WAVE FORMS**



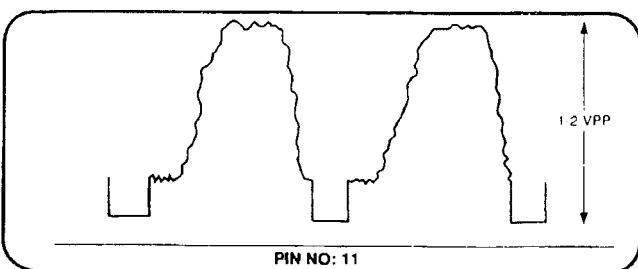
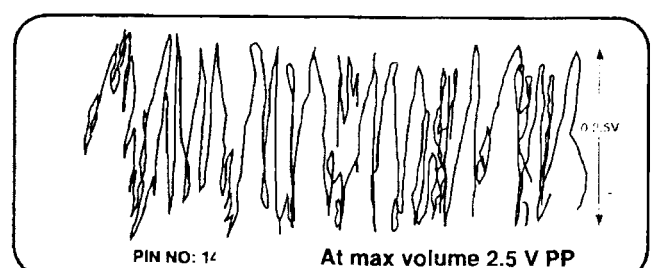
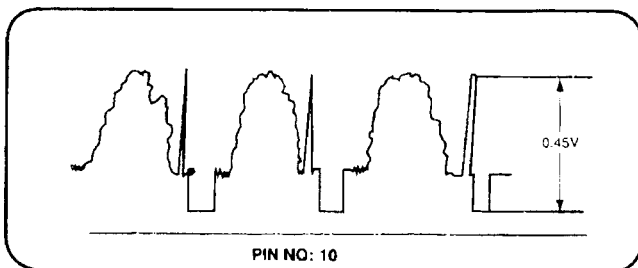
**T551 TRN BC618
OSCILLOSCOPE WAVE FORMS**



IC401 ST6387 OSCILLOSCOPE WAVE FORMS



IC101 STV8223B OSCILLOSCOPE WAVE FORMS



PIN VOLTAGES OF INTEGRATED CIRCUITS

1. SWITCH-MODE CIRCUIT AND IC901 PIN VOLTAGES

IC901 Pin No.	Stand-By Mode			Operation Mode		
	DC (V)	AC	NOTES	DC (V)	AC	NOTES
1	12V			12.7		
2	12.4			12.2		
3	0.2			1.7		
4	—			—		
5	2.8V			3.1V		
6	—			—		
7	—			—		
8	0.1			0.1		
9	—			—		
10	2.6			2.6		
11	2.4			2.4		
12	1.3			0.5		
13	1.8			2.7		
14	2.5			2.5		
15	2.5			2.5		
16	2.5			2.5		
D906	—			13V		

Note1: Before these measurements, check if there is +300 VDC
~+330 DVC at pin 1 of TR901.

Note2: Be careful while making measurements never use cold
chassis while the measurements are being made.

Note3: Use measurement instrument that has high
internal impedance.

2- PIN VOLTAGES OF "STV8223B" IC101 IF FREQUENCY IC.

Pin No.			NOTES
	DC (V)	AC (V)	
1	1.9		
2	4.7		
3	2.5		
4	0		
5	5.9		
6	5.9		
7	4.8		
8	3.8		
9	4.5		
10	2.3		
11	2.5		
12	1.8		
13	0.4		
14	4.4		
15	4.5		
16	4.5		
17	9.2		
18	0		
19	2.9		
20	2.9		
21	3.3		
22	4.0		
23	2.3		
24	0.6		

PIN VOLTAGES OF TRANSISTORS

1- Tuner Band Control Transistors:

Transistor Name	UHF is in use			UHF out of use			UHF is in use			UHF out of use			UHF is in use			UHF out of use		
	B(V)	E(V)	C(V)	B(V)	E(V)	C(V)	B(V)	E(V)	C(V)	B(V)	E(V)	C(V)	B(V)	E(V)	C(V)	B(V)	E(V)	C(V)
T452	4	4.7	4.7	4.5	4.7	0												
T453							4	4.7	4.7	4.7	4.7	0						
T454													4	4.7	4.7	4.7	4.7	0

2- Varicap Voltage Control Transistor

Transistor Name		VHF1		VHF3		UHF	
		Start of Band	End of Band	Start of Band	End of Band	Start of Band	End of Band
T451	E (V)	0	0	0	0	0	0
	B (V)	0.6	0	0.6	0	0.6	0
	C (V)	0	29	0	29	0	29

3- LED Switch transistor

Transistor Name	TV is in Stand- By Mode			TV is Operating		
	E (V)	B (V)	C (V)	E (V)	B (V)	C (V)
T402	1.1	0.5	0	5	2.2	0

4- Reset transistor

Transistor Name	TV is in Stand- By Mode			TV is Operating		
	E (V)	B (V)	C (V)	E (V)	B (V)	C (V)
T403				4.36	3.72	4.35

5- Vertical Output IC (K501) Control Transistors

Transistor No	TV is Normal			Geometry Adjustments are destroyed or there is a defect.			NOTES
	E (V)	B (V)	C (V)	E (V)	B (V)	C (V)	
T 501	0	0.6	0				Measurements are made when the geometry adjustments on the screen are exactly right.
T 502	5.2	5.7	11.5				

6- Horizontal Output Driver Transistor

Transistor No	E (V)	B (V)	C AC (V)	NOTES
T551	—	0.3	9	The measurement that is made while the TV is in normal operation

7- CVBS Driver and Impedance Adapter

Transistor No	E (V)	B (V)	C (V)	NOTES
T101	1.9	0.13	—	

8- External Scart CVBS, Video and Audio Input Control Transistors

Transistor No	E (V)	B (V)	C (V)
T131-BC848B External Sound Control	3.8	4.4	4.8
T130-BC848B External CVBS Control	1.8	2.5	4.8

NOTE: Voltages of T552-BU508DF1 transistor are not given here for safety of your measurement instruments.

9-"Pop" Sound Cutting Circuit While The TV is Being Switched On-Off

Transistor No	E (V)	B (V)	C (V)	NOTES
T302	0	0.65	0	
T301	0	0	0	

**5- PIN VOLTAGES OF SECAM CONVERTER AND DELAY
LINE "STV2180A" IC.**

Pin No.			Pin No.		
	DC (V)	AC (V)		DC (V)	AC (V)
1		0	8		0
2		2.5	9		1.1
3		3.1	10		6.8
4		3.1	11		9.0
5		3.9	12		0
6		0.6	13		0
7		0	14		2.5

6- PIN VOLTAGES OF "STV5112" IC 801 RGB OUTPUT IC.

Pin No.	Function			NOTES
		DC (V)	AC (V) (By oscilloscope)	
1	Blue Input	2.4		
2	Vcc (16 V)	9.0		
3	Green Input	2.5		
4	Red Input	2.5		
5	VDD (+185 V Input)	+185		
6	Red Cathode Current	3.0		
7	Red Output	107		Changes according to the picture
8	Chassis (Ground)	-		
9	Red Feedback	110		Changes according to the picture
10	Green Output	118		Changes according to the picture
11	Green Cathode Current	2.1		
12	Green Feedback	122		Changes according to the picture
13	Blue Output	120		Changes according to the picture
14	Blue Cathode Current	2.2		
15	Blue Feedback	121		Changes according to the picture

3- PIN VOLTAGES OF "ST6387" (IC401) CPU

Pin No.			Pin No.		
	DC (V)	AC		DC (V)	AC)
1	5.0		22	0	
2	1.1		23	0	
3	2.2		24	0	
4	2.2		25	0	
5	0.1		26	0.9	
6	2.1		27	0.2	
7	0		28	4.9	
8	1.3		29	4.9	
9	2.2		30	0	Stops while operating.
10	4.9		31	—	
11	0		32	—	
12	0		33	4.3	
13	4.9		34	2.1	
14	4.9		35	4.9	
15	4.9		36	0	
16	4.9		37	7.9	
17	4.7		38	0.4	
18	4.7		39	1.3	
19	9.2		40	3.8	
20	0		41	2.8	
21	0		42	4.9	

4. PIN VOLTAGES OF (IC 151) "STV2116A" COLOUR AND RGB INPUT/OUTPUT IC.

Pin No.			Pin No.		
	DC (V)	AC (V)		DC (V)	AC (V)
1	0		22	9.2	
2	8.3		23	0	
3	3.8		24	2.2	
4	4.8		25	2.0	
5	3.5		26	2.1	
6	3.8		27	1.9	
7	2.8		28	2.1	
8	4.6		29	1.8	
9	0		30	2.1	
10	0.6		31	6.7	
11	0		32	2.5	
12	1.5		33	4.5	
13	1.4		34	4.5	
14	1.4		35	5.4	
15	0		36	2.9	
16	1.8		37	0.6	
17	1.6		38	2.7	
18	1.6		39	2.9	
19	0		40	5.7	
20	4.0		41	5.6	
21	0		42	9.1	

7- PIN VOLTAGES OF "STV5347" TELETEXT IC.

Pin No.			Pin No.		
	DC (V)	AC (V)		DC (V)	AC (V)
1	0.3		15	0	
2	0		16	2.4	
3	4.9		17	3.7	
4	0		18	0	
5	4.5		19	4.9	
6	0		20	0	
7	0		21	4.9	
8	0.4		22	4.9	
9	0.7		23	2.4	
10	0.8		24	—	Can not be measured passing channel picture
11	4.9		25	0	
12	4.7		26	0	
13	0.2		27	0	
14	24		28	1.2	

8- PIN VOLTAGES OF "TDA2822" (IC301) AUDIO OUTPUT IC.

Pin No.			Pin No.		
	DC (V)	AC (V)		DC (V)	AC (V)
1	0		9	0	
2	0		10	0	
3	0.5		11	5.8	
4	0		12	0	
5	0		13	0	
6	5.8		14	0.5	
7	0		15	0.2	
8	12.8		16	0	

9. VERTICAL OUTPUT STAGE AND "TDA8174A" (IC501) PIN VOLTAGES

Pin No.	Function	Operation Mode	
		DC (V)	AC (V) (By Oscilloscope)
1	Vert. Deflection Output	+ 12V	
2	Output Stage Vs	25V	
3	Trigger Input	5.2	
4	Amplitude	4.6	
5	Vertical Reference	1.5	
6	Chassis		
7	Ramp Generator	4.6	
8	Vert. Amp. Driver	5.6	
9	Inverting Input	4.4	
10	Mains Voltage	25	
11	Flyback Generator	1.1	

IR-RECEIVER / DEMODULATOR DEVICE

- Photodiode with hybride integrated circuit
- Available for several Carrier frequencies
- Black epoxy resin , daylight filter optimized for 950 nm
- High immunity against ambient light
- Low power consumption
- 5 V supply voltage
- High sensitivity (internal shield case)
- TTL and CMOS compatibility
- Continuous transmission possible ($t_{pl} / T \leq 0.4$)

The diagram shows a PIC16C55B-04P microcontroller. Key components include:

- Power Supply:** +3V source connected to pin 24 (VCC) via a pull-up resistor P.R.1.
- Timing Network:** Resistor R1 (0.47M) and capacitor C1 (47uF) connected to pins 23 (OSC) and 22 (OSC).
- IR LED Output:** An IR LED connected to pin 21 (OUT) through a transistor BC337 T1.
- Reset Circuit:** Capacitors C3 (100pF) and C4 (100pF) connected to pins 1 (RESET) and 2 (RESET).
- Peripheral Device:** A large component with multiple pins (e.g., TXE, RX, TXD, RXD, TXEN, RXEN, TXD+, RXD+, TXD-, RXD-) and internal logic blocks like TXE, RXE, TXD+, RXD+, TXD-, RXD-, TXEN, RXEN, TXD+, RXD+, TXD-, RXD-.

SERVICE ADJUSTMENTS

1-Supply Voltage adjustment

Connect a digital voltmeter to the anode of D950 and set the screen potentiometer to minimum. Adjust the main supply voltage +B with P901 to following voltage values;

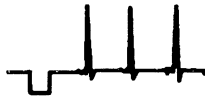
113V DC for 14" IRICO tube,
107V DC for 14" PHILIPS tube,
104V DC for 14" LG tube,
121V DC for 20" SAMSUNG tube,
117V DC for 20" LG tube,
113V DC for 21" LG tube,
119V DC for 21" SAMSUNG tube,

Adjust the screen potentiometer to the level where a picture is just visible. Adjust the focus potentiometer.

2- AFC adjustment

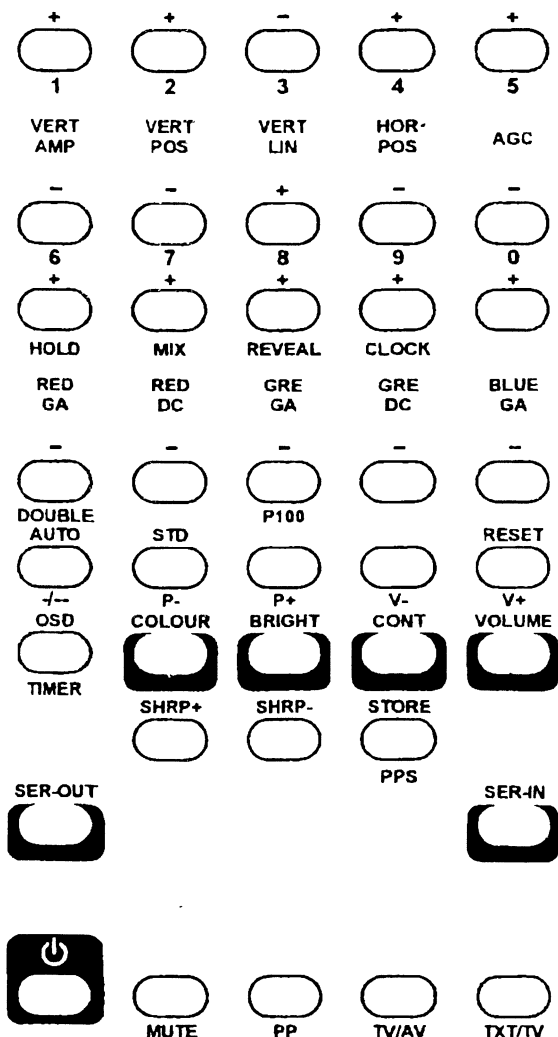
Press Yellow button then TVTX button to call the tuning table. Press Yellow button again to set the AFC to OFF. Apply a crosshatch pattern with 38.9 IF carrier to pins 1-2 of F105. Connect the oscilloscope to the video output pins of the scart connector. Adjust L101 until the waveform on the oscilloscope Fig 1 is visible and the voltage at PIN 9 of IC 401 becomes 2,425 V + - 75mV. Video output level at scart output should be 2Vpp.

Figure 1



Set the AFC ON again in menu.

SERVICE REMOTE CONTROL:



3- AGC adjustment

Apply a signal at CH32 with 60±dBuV level to the antenna input. Enter the Service Mode, using "Ser IN" button on service RC. Using "AGC" buttons adjust the voltage at the AGC pin of Tuner to 4 V + - 50mV DC. Press "PPS" to store the adjusted values.

4- Sharpness adjustment

Set the XY value (sharpness adjustment) to 4 by using 'SHRP + 'and' SHRP - 'buttons on service RC.

Apply an AV signal from Scart (Video in (20) and Audio in (2 and 6)) inputs of CHASSIS and then observe a clear picture and sound.

5- Geometry adjustment

Apply a FUBK or Philips test pattern.
For Vertical Linearity, use buttons "2" and "7".
For Vertical Position, use buttons "3" and "8".
For Vertical Amplitude, use buttons "1" and "6".
For Horizontal Position, use buttons "4" and "9".

There is no Horizontal width adjustment. If this adjustment is necessary this can be done changing the mains voltage ± 1V.

6- Screen adjustment

Set the TV to AV mode when Brightness (%55), Contrast (%80), and Color (%55) are at their stored values. Connect a digital voltmeter to PIN10 of IC801. Adjust the screen potentiometer by increasing the voltage from 0 to 105 ± 1V.

7- White balance adjustment

Apply a Gray Scale test pattern. There is no blue cut-off adjustment (low light) at white adjustment. Set the G-Gain value to 45 using "G-Gain+" and "G-Gain-" buttons. Then perform white adjustment by using, Red high light increase/decrease (R-Gain +/-) buttons. Blue high light increase/decrease (B-Gain +/-) buttons. Red low light increase/decrease (R-DC +/-) buttons. Green low light increase/decrease (G-DC +/-) buttons.

Set the colour system to "Auto" using "P-/STD" button.

OSD colour bars can be seen by using "Timer/OSD" for OSD control.

Always, use "SER.IN" button to enter the Servis Menu and "SER.OUT" button to exit the Servis Menu. In order to store press "STORE" button to store above adjusted values.

See attached table for Geometry and White Balance settings.

SERVICE ADJUSTMENTS

1-Supply Voltage adjustment

Connect a digital voltmeter to the anode of D950 and set the screen potentiometer to minimum. Adjust the main supply voltage +B with P901 to following voltage values;

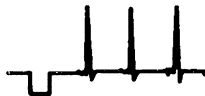
113V DC for 14" IRICO tube,
107V DC for 14" PHILIPS tube,
104V DC for 14" LG tube,
121V DC for 20" SAMSUNG tube,
117V DC for 20" LG tube,
113V DC for 21" LG tube,
119V DC for 21" SAMSUNG tube,

Adjust the screen potentiometer to the level where a picture is just visible. Adjust the focus potentiometer.

2- AFC adjustment

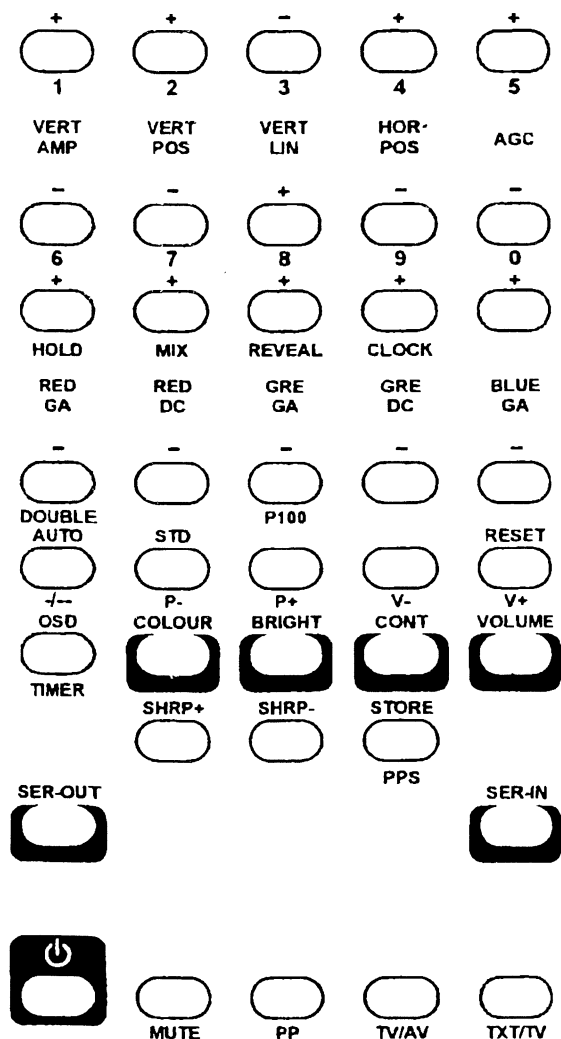
Press Yellow button then TVTX button to call the tuning table. Press Yellow button again to set the AFC to OFF. Apply a crosshatch pattern with 38.9 IF carrier to pins 1-2 of F105. Connect the oscilloscope to the video output pins of the scart connector. Adjust L101 until the waveform on the oscilloscope Fig 1 is visible and the voltage at PIN 9 of IC 401 becomes 2,425 V \pm - 75mV. Video output level at scart output should be 2Vpp.

Figure 1



Set the AFC ON again in menu.

SERVICE REMOTE CONTROL:



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Apply a signal at CH32 with 60 \pm dBuV level to the antenna input. Enter the Service Mode, using "Ser IN" button on service RC. Using "AGC" buttons adjust the voltage at the AGC pin of Tuner to 4 V \pm - 50mV DC. Press "PPS" to store the adjusted values.

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Set the colour system to "Auto" using "P-/STD" button.

OSD colour bars can be seen by using "Timer/OSD" for OSD control.

Always, use "SER.IN" button to enter the Servis Menu and "SER.OUT" button to exit the Servis Menu. In order to store press "STORE" button to store above adjusted values.

See attached table for Geometry and White Balance settings.

ST6387

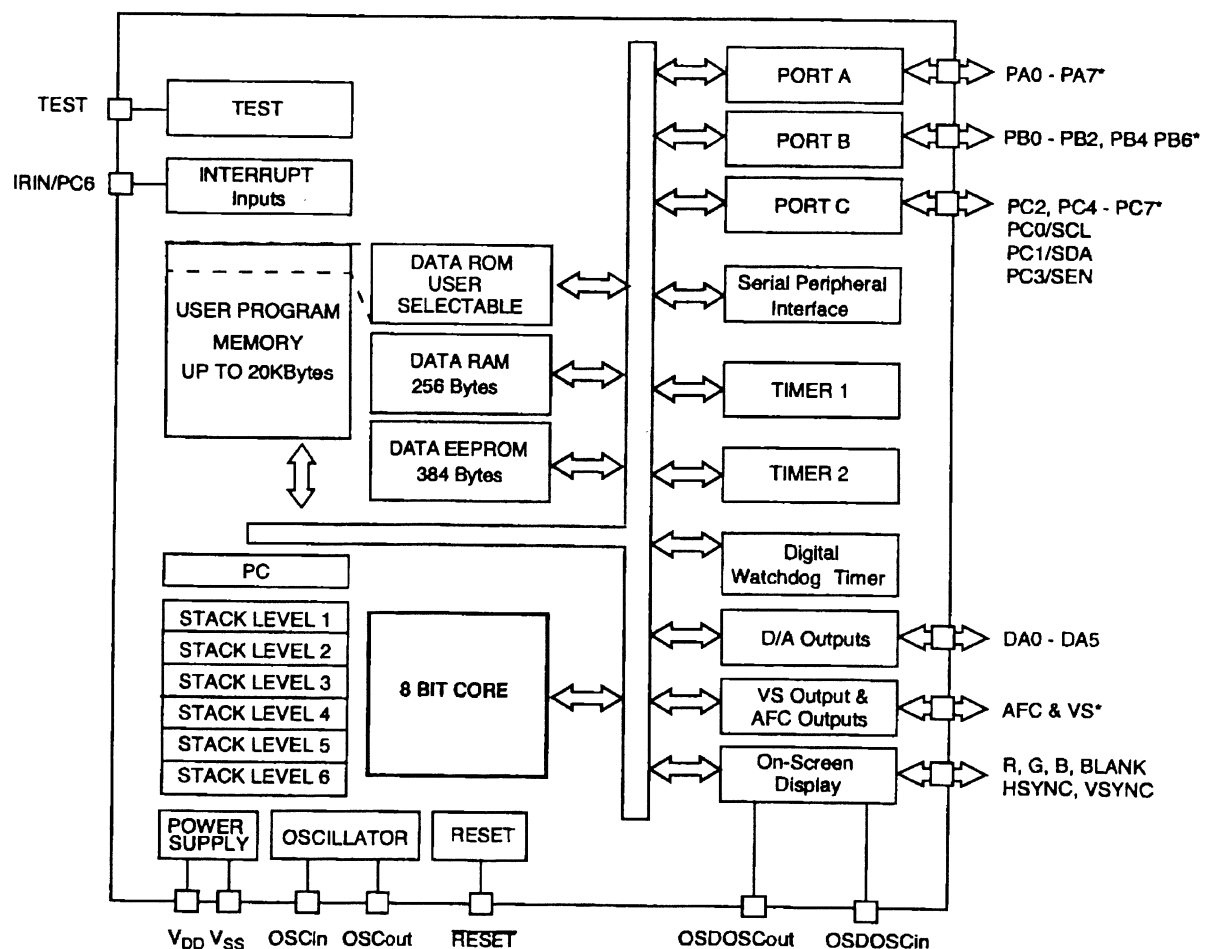
8-BIT MICROCONTROLLER WITH ON-SCREEN-DISPLAY FOR TV TUNING

- 4.5 to 6V supply operating range
- 8MHz Maximum Clock Frequency
- User Program ROM: up to 20140 bytes
- Reserved Test ROM: up to 340 bytes
- Data ROM: user selectable size
- Data RAM: 256 bytes
- Data EEPROM: 384 bytes
- 42-Pin Shrink Dual in Line Plastic Package
- Up to 22 software programmable general purpose Inputs/Outputs, including 2 direct LED driving Outputs
- Two Timers each including an 8-bit counter with a 7-bit programmable prescaler
- Digital Watchdog Function
- Serial Peripheral Interface (SPI) supporting S-BUS/ I²C BUS and standard serial protocols
- SPI for external frequency synthesis tuning
- 14 bit counter for voltage synthesis tuning
- Up to Six 6-Bit PWM D/A Converters
- AFC A/D converter with 0.5V resolution
- Five interrupt vectors (IRIN/NMI, Timer 1 & 2, VSYNC, PWR INT.)
- On-chip clock oscillator
- 5 Lines by 15 Characters On-Screen Display Generator with 128 Characters
- All ROM types are supported by pin-to-pin EPROM and OTP versions.

Device Summary

Device	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	AFC	VS	D/A	Colour Pins	EPROM Devices
ST6387	20K	256	384	Yes	Yes	6	3	ST63E87

Block Diagram



PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCin, OSCout. These pins are internally connected to the on-chip oscillator circuit. A quartz crystal or a ceramic resonator can be connected between these two pins in order to allow the correct operation of the MCU with various stability/cost trade-offs. The OSCin pin is the input pin, the OSCout pin is the output pin.

RESET. The active low RESET pin is used to start the microcontroller to the beginning of its program. Additionally the quartz crystal oscillator will be disabled when the RESET pin is low to reduce power consumption during reset phase.

TEST. The TEST pin must be held at V_{SS} for normal operation.

PA0-PA7. These 8 lines are organized as one I/O port (A). Each line may be configured as either an input with or without pull-up resistor or as an output under software control of the data direction register. Pins PA4 to PA7 are configured as open-drain outputs (12V drive). On PA4-PA7 pins the input pull-up option is not available while PA6 and PA7 have additional current driving capability (25mA, V_{OL}:1V). PA0 to PA3 pins are configured as push-pull.

PB0-PB2, PB4-PB6. These 6 lines are organized as one I/O port (B). Each line may be configured as either an input with or without internal pull-up resistor or as an output under software control of the data direction register.

PC0-PC7. These 8 lines are organized as one I/O port (C). Each line may be configured as either an input with or without internal pull-up resistor or as an output under software control of the data direction register. Pins PC0 to PC3 are configured as open-drain (5V drive) in output mode while PC4 to PC7 are open-drain with 12V drive and the input pull-up options does not exist on these four pins. PC0, PC1 and PC3 lines when in output mode are "ANDed" with the SPI control signals and are all open-drain. PC0 is connected to the SPI clock signal (SCL), PC1 with the SPI data signal (SDA) while PC3 is connected with SPI enable signal (SEN, used in S-BUS protocol). Pin PC4 and PC6 can also be inputs to software programmable edge sensitive latches which can generate interrupts; PC4 can be connected to Power Interrupt while PC6 can be connected to the IRIN/NMI interrupt line.

DA0-DA5. These pins are the six PWM D/A outputs of the 6-bit on-chip D/A converters. These lines have open-drain outputs with 12V drive. The output repetition rate is 31.25KHz (with 8MHz clock).

AFC. This is the input of the on-chip 10 levels comparator that can be used to implement the AFC function. This pin is an high impedance input able to withstand signals with a peak amplitude up to 12V.

OSDOSCin, OSDOSCout. These are the On Screen Display oscillator terminals. An oscillation capacitor and coil network have to be connected to provide the right signal to the OSD.

HSYNC, VSYNC. These are the horizontal and vertical synchronization pins. The active polarity of these pins to the OSD macrocell can be selected by the user as ROM mask option. If the device is specified to have negative logic inputs, then these signals are low the OSD oscillator stops. If the device is specified to have positive logic inputs, then when these signals are high the OSD oscillator stops. VSYNC is also connected to the VSYNC interrupt.

R, G, B, BLANK. Outputs from the OSD. R, G and B are the color outputs while BLANK is the blanking output. All outputs are push-pull. The active polarity of these pins can be selected by the user as ROM mask option.

VS. This is the output pin of the on-chip 14-bit voltage synthesis tuning cell (VS). The tuning signal present at this pin gives an approximate resolution of 40KHz per step over the UHF band. This line is a push-pull output with standard drive.

Pin configuration

DA0	1	42	V _{DD}
DA1	2	41	PC0/SCL
DA2	3	40	PC1/SDA
DA3	4	39	PC2
DA4	5	38	PC3/SEN
DA5	6	37	PC4/PWRIN
PB1	7	36	PC5
PB2	8	35	PC6/IRIN
AFC	9	34	VS
PB4	10	33	RESET
PB5	11	32	OSCout
PB6	12	31	OSCin
PA0	13	30	TEST/V _{PP} ⁽¹⁾
PA1	14	29	OSDOSCin
PA2	15	28	OSDOScout
PA3	16	27	VSYNC
PA4	17	26	HSYNC
PA5	18	25	BLANK
PA6 (HD0)	19	24	B
PA7 (HD1)	20	23	G
V _{SS}	21	22	R

(1) This pin is also the V_{pp} input for OTP/EPROM devices

Pin Summary

Pin Function	Description
DA0 to DA5	Output, Open- Drain, 12V
AFC	Input, High Impedance, 12V
VS	Output, Push- Pull
R, G, B, BLANK	Output, Push- Pull
HSYNC, VSYNC	Input, Pull- up, Schmitt Trigger
OSDOSCin	Input, High Impedance
OSDOSCout	Output, Push- Pull
TEST	Input, Pull- Down
OSCin	Input, Resistive Bias, Schmitt Trigger to Reset Logic Only
OS Cout	Output, Push- Pull
RESET	Input, Pull- up, Schmitt Trigger Input
PA0- PA3	I/ O, Push- Pull, Software Input Pull- up, Schmitt Trigger Input
PA4- PA5	I/ O, Open- Drain, 12V, No Input Pull- up, Schmitt Trigger Input
PA6- PA7	I/ O, Open- Drain, 12V, No Input Pull- up, Schmitt Trigger Input, High Drive
PB0- PB2	I/ O, Push- Pull, Software Input Pull- up, Schmitt Trigger Input
PB4- PB6	I/ O, Push- Pull, Software Input Pull- up, Schmitt Trigger Input
PC0- PC3	I/ O, Open- Drain, 5V, Software Input Pull- up, Schmitt Trigger Input
PC4- PC7	I/ O, Open- Drain, 12V, No Input Pull- up, Schmitt Trigger Input
V _{DD} , V _{SS}	Power Supply Pins

DC ELECTRICAL CHARACTERISTICS

(TA = 0 to +70°C unless otherwise specified).

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V _{IL}	Input Low Level Voltage	All I/O Pins			0.2xV _{DD}	V
V _{IH}	Input High Level Voltage	All I/O Pins	0.8xV _{DD}			V
V _{HYS}	Hysteresis Voltage ⁽¹⁾	All I/O Pins V _{DD} = 5V		1.0		V
V _{OL}	Low Level Output Voltage	DA0-DA5, PB0-PB6, OSD Outputs, PC0-PC7, O0, O1, PA0-PA5 V _{DD} = 4.5V I _{OL} = 1.6mA I _{OL} = 5.0mA			0.4	V
					1.0	V
V _{OL}	Low Level Output Voltage	PA6-PA7 V _{DD} = 4.5V I _{OL} = 1.6mA I _{OL} = 25mA			0.4	V
					1.0	V
V _{OL}	Low Level Output Voltage	OSDOSCout OS Cout V _{DD} = 4.5V I _{OL} = 0.4mA			0.4	V
V _{OL}	Low Level Output Voltage	VS Output V _{DD} = 4.5V I _{OL} = 0.5mA I _{OL} = 1.6mA			0.4	V
					1.0	V
V _{OH}	High Level Output Voltage	PB0-PB7, PA0-PA3, OSD Outputs V _{DD} = 4.5V I _{OH} = - 1.6mA	4.1			V
V _{OH}	High Level Output Voltage	OSDOSCout, OSCout, V _{DD} = 4.5V I _{OH} = - 0.4mA	4.1			V
V _{OH}	High Level Output Voltage	VS Output V _{DD} = 4.5V I _{OH} = - 0.5mA	4.1			V
I _{PU}	Input Pull Up Current Input Mode with Pull-up	PB0-PB6, PA0-PA3, PC0-PC3, V _{IN} = V _{SS}	- 100	- 50	- 25	μA
I _{PU}	Input Pull Up Current	OSCin V _{IN} = V _{SS}	- 50	- 25	- 10	μA
I _{IL} I _{IH}	Input Leakage Current	OSCin V _{IN} = V _{SS} V _{IN} = V _{DD}	- 10 0.1	- 1 1	- 0.1 10	μA
I _{IL}	Input Pull-down current in RESET	OSCin	100			μA
I _{IL} I _{IH}	Input Leakage Current	All I/O Input Mode no pull-up OSDOSCin V _{IN} = V _{DD} or V _{SS}	-10		10	μA
V _{DD} RAM	RAM Retention Voltage in RESET Mode		1.5			V
I _{IL} I _{IH}	Input Leakage Current	Reset Pin with Pull-up V _{IN} = V _{SS}	- 50	- 30	- 10	μA

14 11

Do not insert for UHF only chassis!

UV1315 TU001

SECAM L L'

STV8223B (STV 8224B for SEC LL')

ST6387B1/F10 IC401

MC44603AP IC901

Subject to change without notice

D401: UHF ONLY TUNER
D403: BACKGROUND FREE OSD
D411: AV2
D406: SEC L/L'

OSD_LANG_ENGLISH: D404
OSD_LANG_FRENCH : D404 and D405
OSD_LANG_GERMAN : D405

*Operation Range 105VAC~270VAC: R910= 47K; R922=470K; C908=68uF
 Operation Range 140VAC~270VAC: R910=120K; R922= -- ; C908=47uF

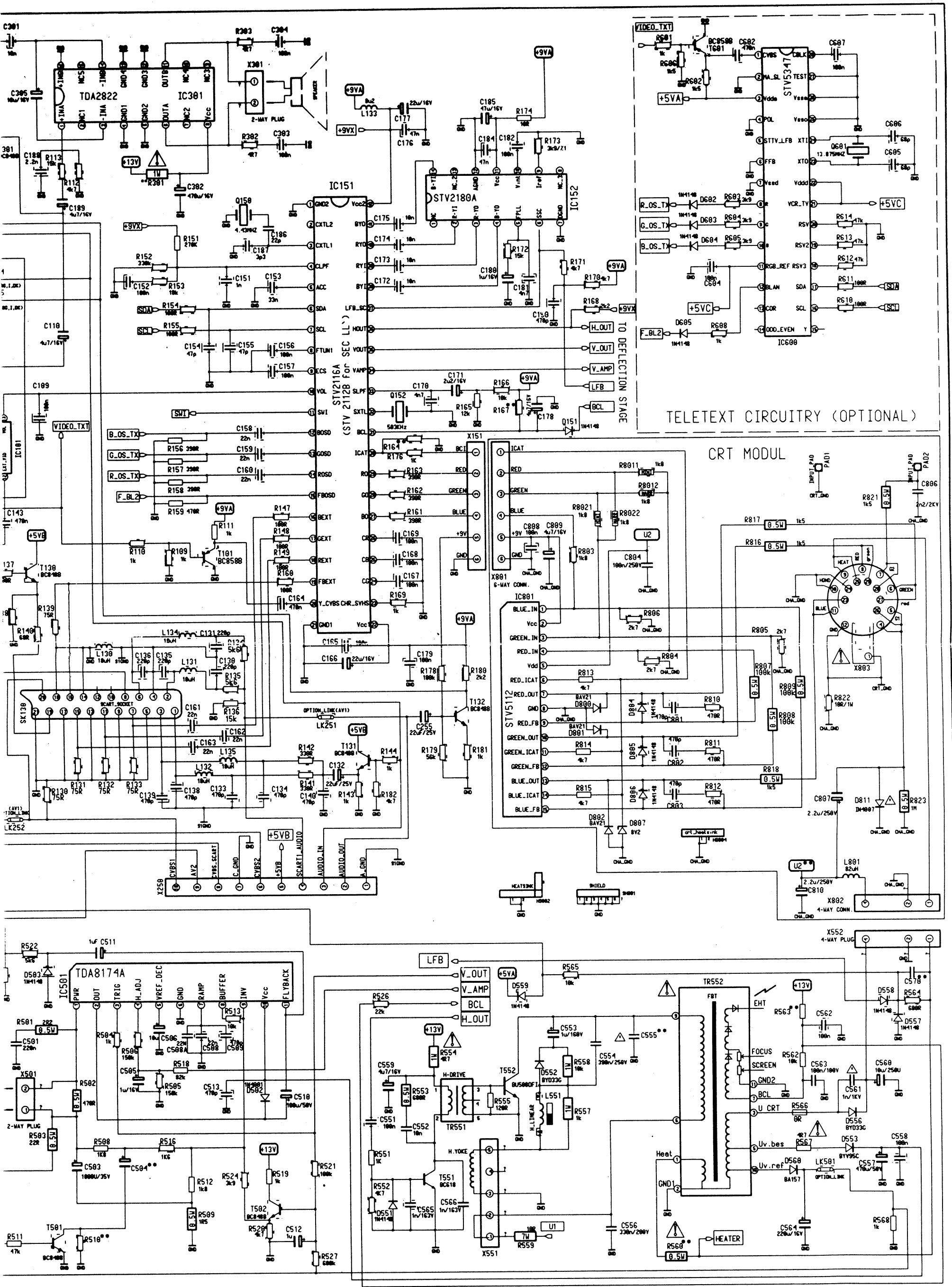
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** 14" SAMSUNG CPT: U1=108V; R5
   14" LG CPT: U1=104V; R5
   14" PHILIPS CPT: U1=107V; R5
   14" IRICO CPT: U1=113V; R5
   20" SAMSUNG CPT: U1=121V; R5
   20" LG CPT: U1=117V; R5
   21" SAMSUNG CPT: U1=119V; R5
   21" LG CPT: U1=113V; R5

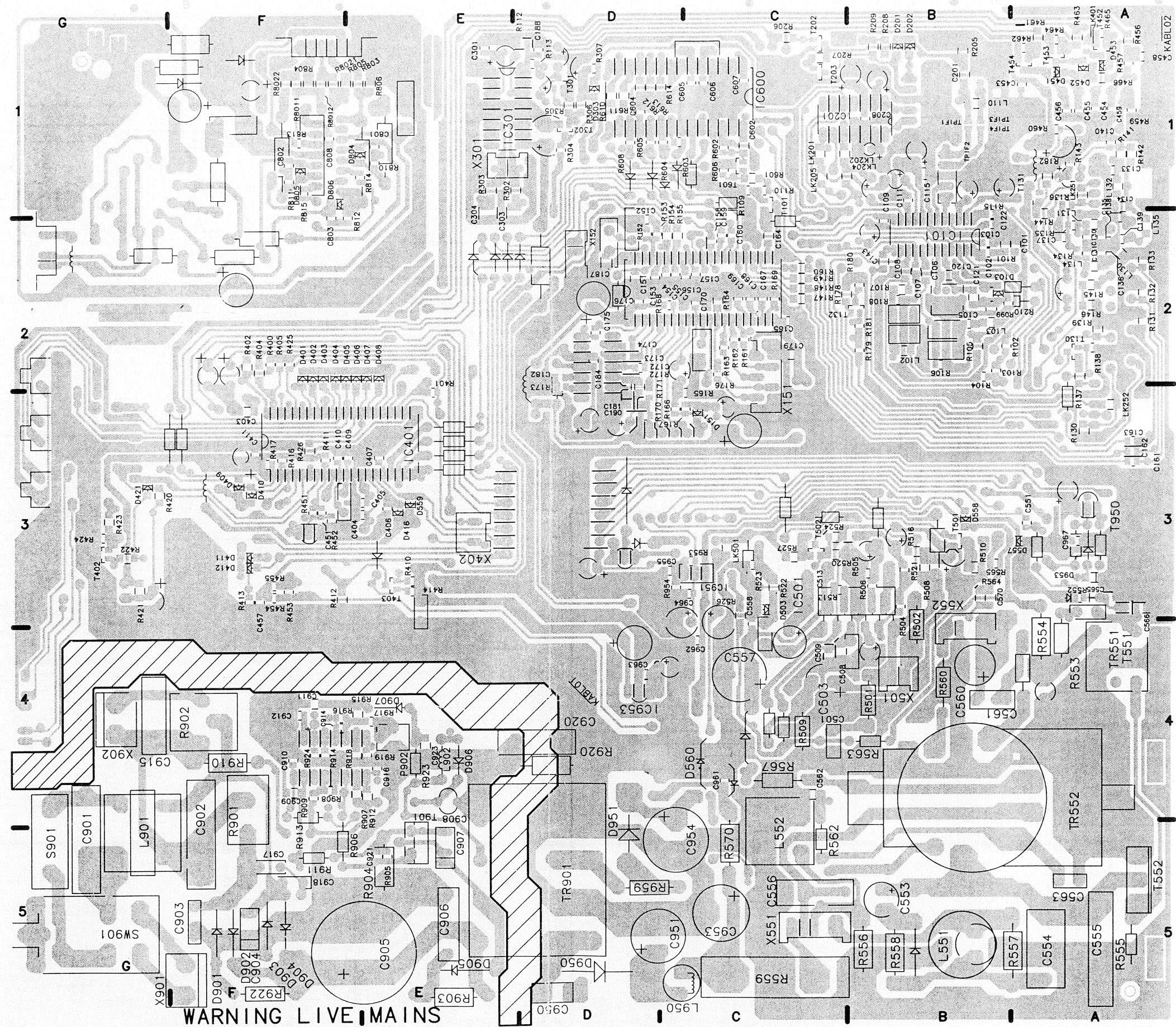
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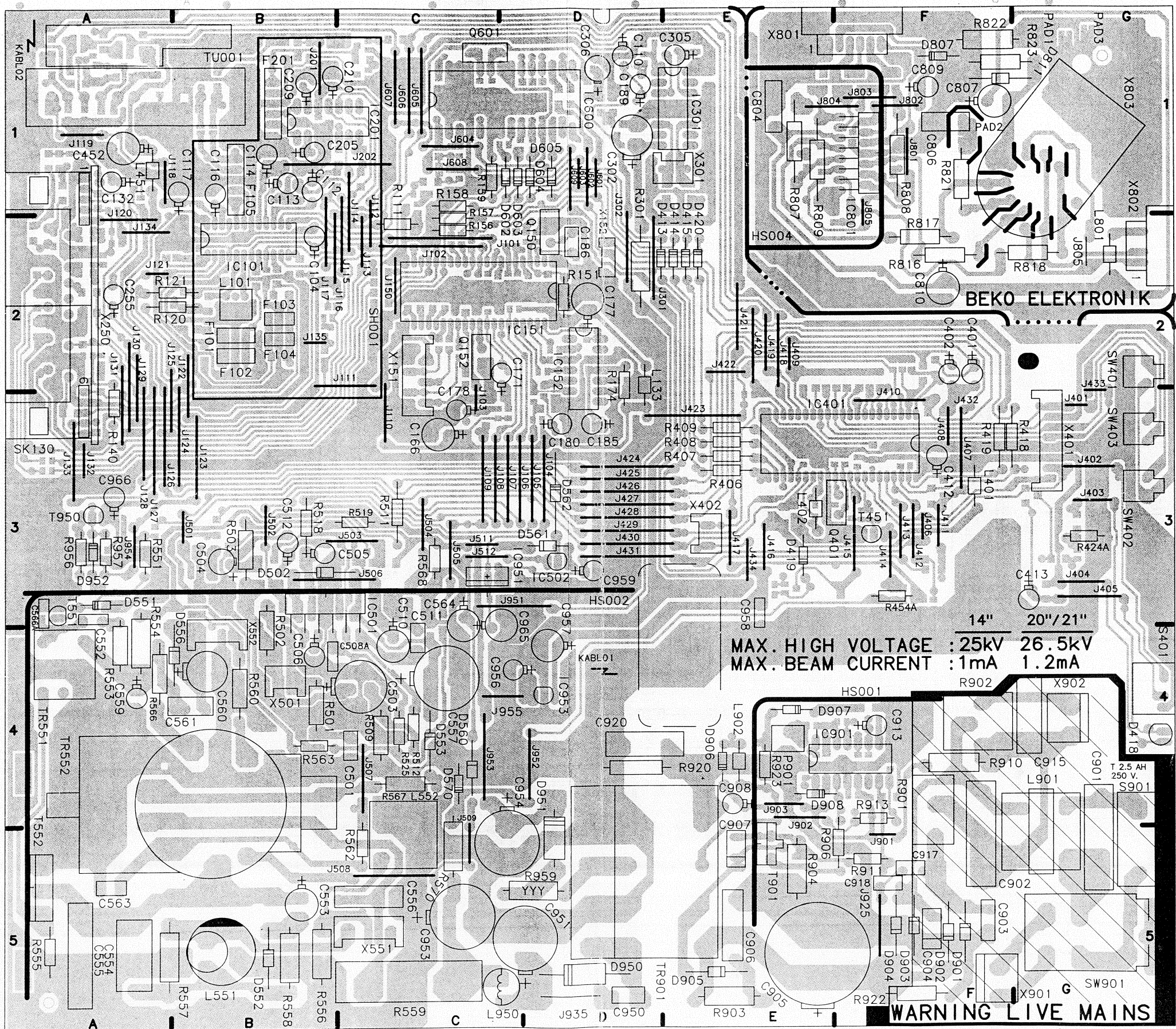
EMC related components: C130,C131,C,133,C134,C135,C136,C138,C139

144 Crown CTV 7216



SUNC CPT: U1=108V; R510=150R; R560=1R2; R563=8k2; C504=100uF; C555=6n8F; R164=47k; R167=220k; U2=185V; P901=1k5; R527=open; R301=3R3; C570=open
 CPT: U1=104V; R510=150R; R560=1R2; R563=8k2; C504=100uF; C555=6n8F; R164=47k; R167=220k; U2=185V; P901=1k5; R527=680k; R301=3R3; C570=open
 IPS CPT: U1=107V; R510=150R; R560=1R2; R563=8k2; C504=100uF; C555=6n8F; R164=47k; R167=220k; U2=185V; P901=1k5; R527=680k; R301=3R3; C570=open
 CO CPT: U1=113V; R510=150R; R560=1R2; R563=8k2; C504=100uF; C555=6n8F; R164=47k; R167=220k; U2=185V; P901=1k5; R527=680k; R301=3R3; C570=open
 SUNC CPT: U1=121V; R510=100R; R560=R47; R563=6k8; C504=220uF; C555=9n1F; R164=10k; R167=100k; U2=220V; P901=2k2; R527=680k; R301=2R2; C570=10nF
 CPT: U1=117V; R510=100R; R560=R47; R563=6k8; C504=220uF; C555=8n2F; R164=10k; R167=100k; U2=220V; P901=2k2; R527=680k; R301=2R2; C570=10nF
 SUNC CPT: U1=119V; R510=100R; R560=R47; R563=6k8; C504=220uF; C555=8n2F; R164=8k2; R167=100k; U2=220V; P901=2k2; R527=680k; R301=2R2; C570=10nF
 CPT: U1=113V; R510=100R; R560=R10; R563=6k8; C504=220uF; C555=8n2F; R164=8k2; R167=100k; U2=220V; P901=2k2; R527=680k; R301=2R2; C570=10nF





Force FT3886 + SFE

Power 22
Univision
FX 818

Ch. 12.1
Crown CTV 9216